Performance of Channel Engineered SDODEL MOSFET for Mixed Signal Applications

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Abstract- In this paper, with the help of simulations the concepts of source/drain (S/D) impurity profile engineering are proposed for reduction of the junction capacitance (Cj). It has been recently shown that it is possible to realize the benefits of PD- SOI technologies with the help of Source/Drain On Depletion Layer (SDODEL) MOSFETs, employing the bulk technologies. Here, for the first time, we investigated analog performance improvement with Single Halo SDODEL MOSFETs, as well as Double Halo SDODEL MOSFET and compared their performances with Double Halo MOSFETs (which will henceforth be referred as Control MOSFETs) with extensive process and device simulations. Our results show that, in Single Halo SDODEL MOSFET there is a significant improvement in the intrinsic device performance for analog applications (such as device gain, g_m/I_D etc.) for sub 100nm technologies.

I. Introduction

Silicon–on-insulator (SOI) devices are very attractive for high performance ULSI technologies. SOI devices offer interesting features such as reduction of junction capacitance and increase of packing density (compared with bulk devices), suppression of latch up and reduction of short channel effects. However there are many disadvantages associated with SOI devices, such as wafer quality and cost, self heating and additional body contact area. SOI technology employing partially depleted transistor suffers from floating body effects and dependence of gate delay on device switching history. In recent past pseudo SOI technologies were developed [1], [2] on bulk substrate to realize reduced junction capacitances without the disadvantages associated with PD SOI.

The pseudo SOI technology first proposed in [1] referred as "Pseudo-SOI" (p-SOI) features a p-n-p channel profile, in which the sandwiched n-type layer is fully depleted by the internal built-in-potential. The depletion region established beneath the channel, source and drain regions electrically isolates the channel region from the substrate region and works as an insulator similar to buried oxide (BOX) in SOI.

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In Pseudo-SOI MOSFETs the significantly increased depletion volume may lead to increased generation current and cross talk and the continuous depletion region beneath the channel may result a higher S/D leakage in nano regime. A similar idea developed by [2] referred as "SODEL" with an epitaxial silicon layer is employed to form a thin channel layer over the depletion layer to suppress short channel effects at the expense of increased process cost and complexity. In the pseudo SOI technology developed by [3], referred as SDODEL, a high energy, low dose implant of the source /drain (S/D) doping type is introduced after the gate definition step to form depletion layer, by counter doped regions beneath the source and drain. The idea behind this is to develop a low cost alternative to PD SOI. In the case of SDODEL transistors only an additional counter doping implant is required which makes fabrication process less complex than the SODEL approach, wherein two additional steps, a counter doped implant and an epitaxial growth are required.

In this work we have investigated analog performance parameters in Single Halo SDODEL MOSFET (SH SDODEL), Double Halo SDODEL MOSFET (DH SDODEL) and compared them with control MOSFETs using extensive process and device simulations. Device simulation results show that a further reduction of junction capacitances can be achieved with the help of Double Halo SDODEL MOSFETs as compared to the Single Halo SDODEL MOSFET and the Control MOSFETs. In Single Halo SDODEL MOSFET there is significant improvement in the intrinsic device performance for analog applications (such as device gain, g_m/I_D etc.) for the sub 100nm technology nodes.

II. Simulation Setup

In this section the structures of control, SH SDODEL and DH SDODEL MOSFET are discussed. Standard MOS fabrication process flow was followed for all the devices. In case of control MOSFET (DH devices), the process flow is identical to that of conventional MOSFETs except for the threshold adjust implant, which is done through a tilted angle implantation from both the source and drain sides after the gate electrode formation. Here, the pocket regions have been realized using Boron for the n-channel MOSFETs at a tilt angle of 15^0 and 0^0 wafer orientations. For SDODEL device, an additional high energy and low dose S/D implant is introduced during the deep S/D implant to form the counter-doped regions. We have introduced Arsenic for this implant in the n-channel transistors. The standard threshold adjust implant has been

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done with BF_2 for SDODEL device. In case of SH SDODEL MOSFET, tilted angle implantation is done from the source side to realize the pocket only on the source side. All the 2D simulations have been carried out using ISE TCAD [4]. DIOS is used for process simulations and DESSIS is used for device simulations. Energy balance models are used for device simulations in order to account for the non-local effects. In order to take surface quantization effects into account, Van-Dort's model is used for device simulation. For both CONTROL and SDODEL devices, the implantation dose is adjusted to achieve identical V_T as per the SIA roadmap as given in Table I.

TABLE-I
TECHNOLOGY PARAMETERS AND VOLTAGE SCALING USED FOR DEVICE SIMULATIONS

L_g (μm)	0.25	0.18	0.13	0.1	0.07
V_{DD}(V)	2.5	1.8	1.5	1.2	0.8
T_{OX}(nm) Analog	5	4	3.5	3	3
V_T(V) Analog	0.45	0.4	0.35	3	3
V_{DS}(V)	1.25	0.9	0.75	0.6	0.4
T_{OX}(nm) Digital	3	2.5	2	1.5	1.2
V_T(V) Digital	0.35	0.3	0.25	0.2	0.2
X_j(nm)	65	50	40	30	25

III. RESULTS AND DISCUSSION

A. Reduction in Junction Capacitance C_j – The simulated junction capacitance C_j of n-channel Control, SH SDODEL and DH SDODEL devices as a function of drain-body bias V_{DB} for two different T_{ox} values of 1.5 and 3.0nm are shown in Fig.1 and 2 respectively. In comparison with control devices, both DH and SH SDODEL devices show more than 42% reduced junction capacitance C_j for T_{ox}=1.5nm at a bias voltage equal to the supply voltage V_{DD}. For T_{ox}=3nm, DH SDODEL and SH SDODEL devices show more than 40% and 30% reduced junction capacitance C_j respectively for similar bias conditions as stated above.

B. Comparable Sub-threshold Characteristics-

We observed that there is reduction in V_t for the SDODEL devices, which may be due to a slight reduction in the average doping concentration below the channel region due to lateral diffusion of the counter doping implant. The standard threshold adjust implant has been done with BF_2 for the SDODEL devices. Fig.3 and 4 show the sub-threshold characteristics for the n-channel Control, SH SDODEL and DH SDODEL devices with two different T_{ox} values of 1.5 and 3.0nm respectively. The sub-threshold swing of the SDODEL devices is comparable to that of the control devices as seen in Fig.3 and 4 respectively.

C. Transconductance Generation Factor,(g_m/I_D) and Output Resistance (R_o)

The g_m/I_D and R_o are important device performance parameters for analog circuits. The g_m/I_D ratio can be viewed as a figure of merit for the device, since the transcondutance represents the amplification delivered by the device and drain current represents the power dissipation to obtain the amplification. Therefore, the higher the g_m/I_D ratio, the more suitable is the device for analog performance. Low g_m/I_D values correspond to strong inversion operation and high values to weak inversion.

In Fig.5 and 6, we have shown the effect of gate overdrive voltage on the g_m/I_D and R_o respectively at a drain bias of 0.6V for devices with L_G=0.1μm and T_{ox} of 3nm with the other parameters chosen as per the SIA roadmap. It can be observed that, SDODEL devices in the forward mode of operation consistently outperform the control devices at all different gate overdrive voltages. Reduced Drain Induced Barrier Lowering (DIBL) contributes towards the improvement in the output resistance (R_o).

D. Device Intrinsic Gain

In Fig.7 we have shown the plot of the device intrinsic gain as a function of the gate overdrive voltage. Here one can observe that best gain is obtained in the SH SDODEL devices for V_{GT}< 0.4V. The SDODEL devices show a lower gain than the control devices when gate overdrive voltage crosses 0.5V because of fall in g_m. It is getting reduced in SDODEL when V_{GT} is above 0.4V i.e V_{GS} is above 0.7V because of reduction in mobility in the channel region. This is due to the additional channel implant BF_2 by which we are making for V_T adjustment. This can be minimized by optimizing additional implant dose.

E. V_T roll-off and I_{ON}/I_{OFF}

Fig.8 shows the V_T roll-off for the devices with oxide thickness of 1.5 and 3nm with identical V_T for Control and SDODEL devices at L_G=0.1μm. It is observed that for T_{ox}=3nm, below 0.13 technology node better roll-up is achievable in the case of SDODEL devices. From Table-II A and B, we observe that I_{OFF} is less for SH SDODEL MOSFETs in comparison with the other two devices for the two different technology nodes, studied in this work. Fig.9 shows the I_{ON}/I_{OFF} as a function of channel length L_G for the devices scaled as per the digital logic roadmap shown in Table I. It can be observed that the I_{ON}/I_{OFF} increases with an increase in the channel length which is as expected. I_{OFF} was taken at V_{GS}=0V, V_{DS}=V_{DD} for the respective technology node.

TABLE-II.A
I_{OFF} –ANALOG ROADMAP

Sl No.	L_G	Control	DH SDODEL	SH SDODEL
1.	0.1	13.947985 nA/μm	11.000258 nA/μm	10.812372 nA/μm
2.	0.13	1.4762438 nA/μm	1.180523 nA/μm	1.0469652 nA/μm

TABLE-II.B
I_{OFF} - DIGITAL ROADMAP

Sl No.	L_G	Control	DH SDODEL	SH SDODEL
1.	0.1	42.08422 nA/ μm	40.674714 nA/ μm	34.765117 nA/μm
2.	0.13	9.3821391 nA/μm	9.0795684 nA/μm	4.8293959 nA/μm

IV. CONCLUSION

Halo SDODEL MOSFETs were optimized with the help of simulations for the sub 100nm technology nodes. Remarkable reduction in junction capacitance was observed. Better analog performances were observed in the case of SH SDODEL MOSFET. As has been shown, these technologies are suitable where the high cost of the SOI technologies is unacceptable. SH SDODEL MOSFET can therefore be a potential player in the future.

ACKNOWLEDGEMENT

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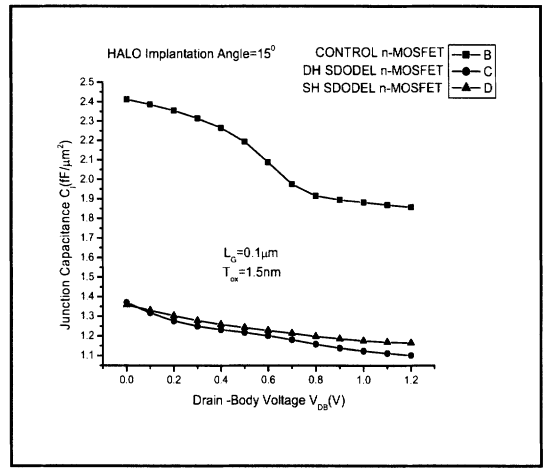

Fig.1- Junction Capacitance C_j as a function of Drain Body Bias V_{DB} for Control and SDODEL MOSFET with T_{OX}=1.5nm.

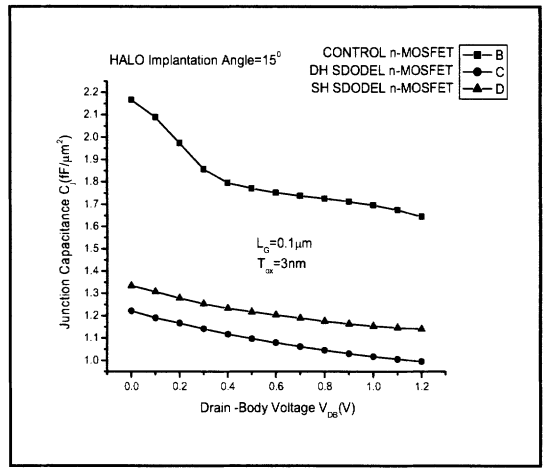

Fig.2- Junction Capacitance C_j as a function of Drain Body Bias V_{DB} for Control and SDODEL MOSFET with T_{OX}=3nm

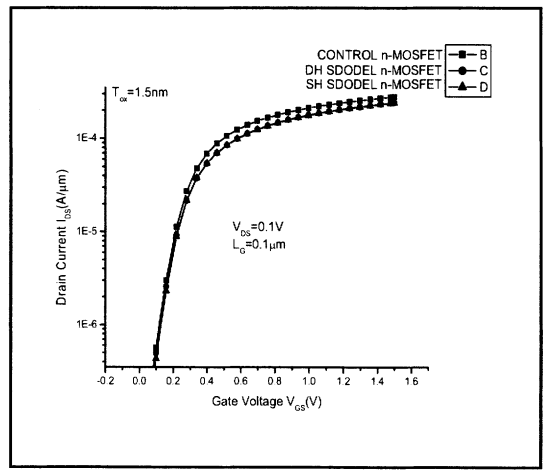

Fig.3. Comparable Sub-threshold Characteristics of Control and SDODEL MOSFET with T_{OX}=1.5nm.

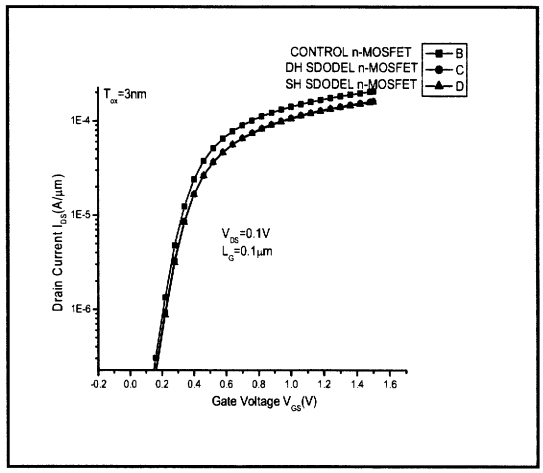

Fig.4. Comparable Sub-threshold Characteristics of Control and SDODEL MOSFET with T_{OX}=3nm.

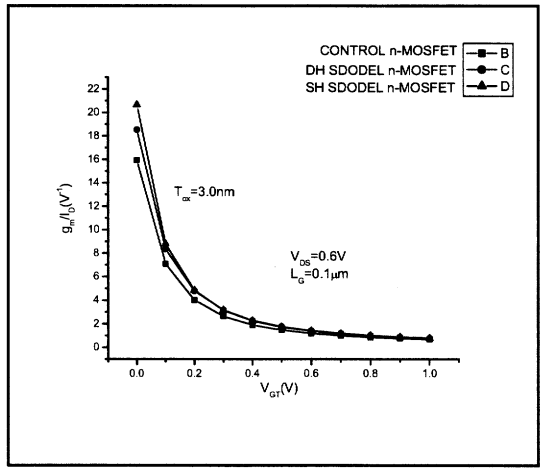

Fig.5.Transconductance generation factor (g_m/I_D) as a function of V_{GT} for CONTROL and SDODEL Transistors with W=1μm, at a drain bias of 0.6V.

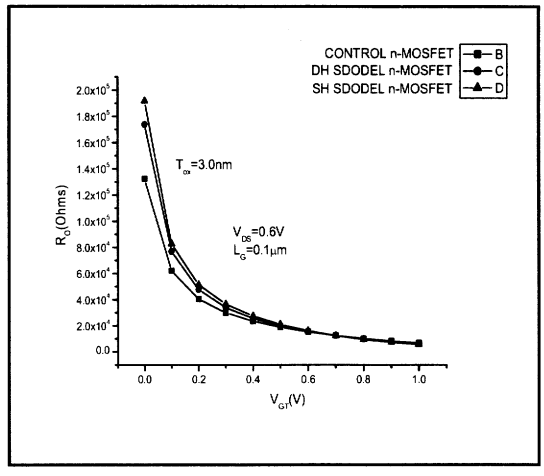

Fig.6.Device Output Resistance (R_O) as function of V_{GT} for CONTROL and SDODEL transistors with W=1μm, at a drain bias of 0.6V.

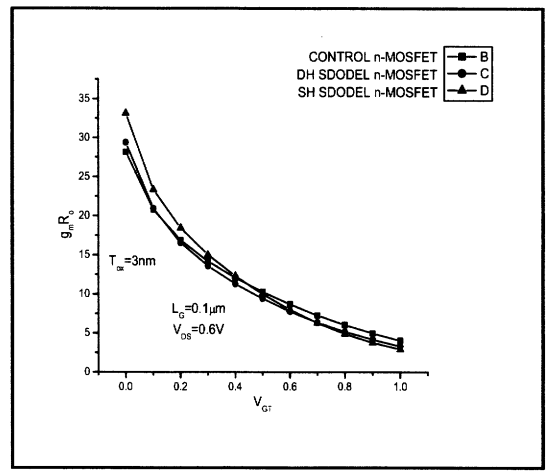

Fig.7. DC intrinsic gain for CONTROL and SDODEL MOSFETs as a function of V_{GS}.

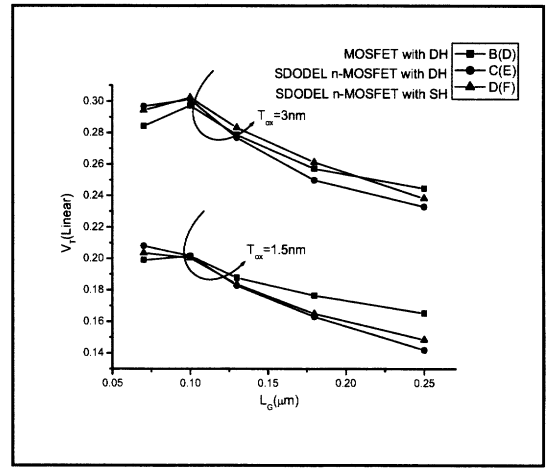

Fig.8. V_T roll-off as function of gate length

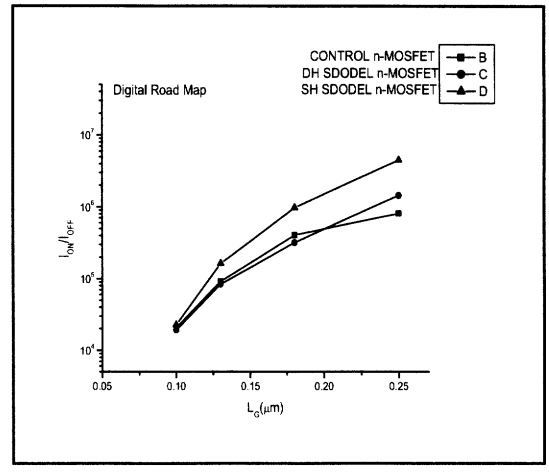

Fig.9. I_{on}/I_{off} as a function of gate length for both CONTROL and SDODEL MOSFETs. V_T is calculated at V_{DS}=100mV.The oxide thickness and V_T are scaled for according to SIA Logic roadmap as given in Table1.