Abstract—In this paper, we describe the application of gate-induced-dRAIN-leakage (GIDL) current for the characterization of gate edge damage which occurs during the plasma etch processes. We show from experimental and simulation results that when the channel is biased in accumulation and with the drain-substrate junction reverse biased, charge injection is localized in the gate–drain overlap region. Under this localized charge injection (LCI) mode of operation, the gate voltage is a function of edge oxide thickness which in turn can be related to the plasma damage received during the poly-etch and subsequent spacer oxide formation. The detailed mechanism of localized charge injection for a study of plasma edge damage is explained along with the experimental demonstration of this technique using submicron MOSFETs.

Index Terms—Charge injection, GIDL, plasma damage, reliability, submicron MOSFETs.

I. INTRODUCTION

The present day ULSI processing heavily utilizes plasma processes because of the requirements of anisotropic etching with high sensitivity and etch rates. Damage can occur to the gate oxide during plasma etching. The main type of damage which has been discussed widely in literature is plasma charging damage [1]–[3]. The term charging damage refers to the degradation of the quality of the gate oxide in a MOS structure due to current flow through the gate oxide in the presence of high electric field by Fowler–Nordheim (FN) tunneling. The imbalance between the ion and electron currents when the gate is placed in a nonuniform plasma causes the FN current [4]. The flow of this tunneling current in the presence of high electric field causes damage to the gate oxide by filling existing electron/hole traps and by breaking bonds to generate new oxide traps and interface states. Plasma charging damage is usually characterized by using antenna structures [5]–[6]. Antenna is a conducting surface connected to the gate and the damage is usually proportional to this conducting surface area.

Another type of damage in MOS transistors which occurs during the poly silicon etching step and subsequent spacer oxide formation is the gate edge damage [7]–[8]. Not much work has been done in understanding the gate edge damage in MOS transistors mainly because of the difficulty in characterizing such a damage. In this work a direct experimental technique will be presented for characterization of edge damage due to plasma processing in submicron MOSFET’s. Experimental and two-dimensional (2-D) device simulation results will be presented to understand the mechanism and to demonstrate the applicability of this technique for the study of plasma edge damage in deep submicron MOSFET’s. In contrast to the plasma charging damage, the edge damage does not anneal out even at high temperatures, leaving parameters of fullyprocessed devices significantly deteriorated [9].

II. LOCALIZED CHARGE INJECTION

We propose a technique called localized charge injection (LCI) for characterization of edge damage in MOSFET’s. This localized charge injection is achieved using a combination of gate and drain voltages, at which the channel region is accumulated and the drain-substrate junction reverse biased. Under sufficiently large drain-to-gate voltage \(V_{DG}\) charge injection occurs only in the gate–drain overlap region. The band diagrams depicting the possible mechanisms responsible for localized charge injection under high drain voltage condition in NMOS and PMOS transistors are shown in Fig. 1. In Fig. 2 is shown the measured gate voltage required to inject a constant gate current, as a function of the drain voltage. Two distinct regions of injection can be noticed in this figure. For low drain voltages, because the lateral electric field is low, the gate voltage required to inject a constant gate current remains constant with respect to the drain voltage. In this mode, FN injection of carriers through the complete gate area occurs and the gate voltage needed for constant current injection remains constant with respect to the drain voltage. This regime of drain voltage is defined as the uniform FN injection regime. At high

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Fig. 1. Band diagrams and the possible mechanisms for LCI under high $V_{dd}$ voltages in NMOS and PMOS transistors.

Fig. 2. $V_{gs}$ dependence of the gate voltage required to maintain constant gate current conditions in NMOS devices with different oxide thickness.

Fig. 3. The drain voltage dependence of transistor currents in the GIDL regime for (a) NMOS and (b) PMOS transistors.

$V_d$, the charge injection occurs exclusively in the gate–drain overlap region, and the gate voltage required in this regime decreases as $V_d$ is increased, to maintain a constant LCI gate current. This is because, at high $V_d$ voltages, there is impact generation in the gate–drain overlap region due to the high lateral electric field and these impact generated carriers get injected into the gate and contribute for the gate current. Hence the gate voltage required for constant gate current injection decreases with increasing drain voltages as seen in Fig. 2. This regime of drain voltage is therefore referred to as LCI mode. In Fig. 3 we show the drain current as a function of increasing drain voltage for both NMOS and PMOS transistors when the channel is biased in accumulation. From Figs. 2 and 3, it is therefore clear that, when monitored under constant gate current conditions, the injection switches from the uniform FN mode to the LCI mode when impact ionization starts in the depleted region at the interface and $V_a$ starts to decrease as $V_d$ is increased. This can be seen in Fig. 3, because the gate current starts to flow only when the drain voltage exceeds values required for impact ionization in the channel region. These impact generated carriers are also responsible for the resulting source and drain currents. The lateral electric field is therefore important for the LCI, which is not a parameter in the case of conventional uniform FN injections through the gate oxide. In Fig. 4 we show the 2-D device simulations performed for an NMOSFET under LCI bias conditions. Impact ionization, band-to-band tunneling, lucky electron, and...
FN tunneling models were used for simulations as supported by ATLAS [10]. The simulations show clearly that under specific bias conditions, electric field and therefore the impact ionization are localized to the gate–drain overlap region which can be used to achieve LCI in the gate–drain overlap region. Further, in the LCI mode the resulting gate current polarity is negative for NMOS and positive for PMOS as observed from both experimental and simulation results. This indicates that gate current is essentially consisting of hole current in the case of NMOS and electron current in the case of PMOS. It should be noted from Fig. 3 that source current has the same polarity as the drain current in the LCI mode i.e., for NMOS devices electrons, which are generated by impact ionization in the gate–drain overlap region, are collected by the source. In other words, both the source current and the drain current are due to electrons flowing out of the source and drain terminals. In Fig. 5 we show the $I_D$, $I_G$, and $I_S$ as a function of $V_D$ in NMOS and PMOS transistors with differing channel lengths. It can be clearly seen from this figure that the source current in the LCI regime decreases with increasing channel lengths indicating a larger recombination of generated carriers during their transit to the source. Since the currents $I_D$ and $I_G$ are caused by the impact generation in the gate–drain overlap region, they are independent of the channel length, as expected.

### III. APPLICATION OF LCI TECHNIQUE FOR DEVICE DIAGNOSTICS

Due to the polysilicon reoxidation step, the thickness of the gate oxide is greater at the edge of the channel than in the mid-channel region. This can be seen in Fig. 6 where a TEM cross section of a 0.5-$\mu$m MOSFET is shown. The edge oxide thickness is significantly higher than the nominal oxide thickness of 9 nm at the center of the device. The amount of oxide thickening during the poly-Si reoxidation step is related to the edge damage at the preceding poly-Si etching step. This edge damage is strongly localized because, during the etch process, the only region of Si–SiO$_2$ active area exposed to the plasma is the region adjoining the channel ends, i.e.
LDD regions and the oxide above them. As a result, the silicon and the oxide may be structurally damaged with the creation of electron/hole traps and the interface significantly degraded. Devices which undergo greater edge damage during poly-Si etching experience enhanced edge oxide thickening during the poly-Si reoxidation step, as shown schematically in Fig. 7. Therefore, if we have a technique to monitor the edge oxide thickness electrically, then we have a method to estimate the edge damage. The Localized Charge Injection technique therefore comes in handy for such a study.

The voltage required for uniform FN injection through the complete gate oxide area has been used as a monitor of nominal gate oxide thickness. Similarly, the voltage required for a charge injection that is localized to the gate–drain overlap region can be used as a measure of the oxide thickness at the gate edge. The gate voltage in the LCI regime required to force a constant gate current through the gate overlap region is a sensitive measure of the edge oxide thickness and in this work it is called the “edge oxide thickening parameter” and will be referred to as “LCI $V_g$” in the rest of the paper. LCI $V_g$ as explained earlier can be used as a measure of plasma edge damage during poly-Si etching. A larger LCI $V_g$ corresponds to a larger edge oxide thickness. If the poly-Si etching is more aggressive, then the actual gate lengths are smaller, and the amount of edge damage is also greater. To verify this, a ten-wafer split was fabricated wherein the wafers underwent poly-Si etching in the same plasma etcher, but under different plasma conditions (magnetic field, power, temperature, and over etch time). The ten wafers have therefore undergone varying levels of plasma edge damage. SEM measurements were performed on special poly-Si lines, with the same nominal width as the gate length (0.35 μm), on the different wafers in the split, to determine their actual dimensions. The plot of the width of these poly-Si lines versus LCI $V_g$ for NMOS devices is shown in Fig. 8. This plot shows the general trend, in which the wafers which have narrower poly lines due to more aggressive etching have increased LCI $V_g$ indicating enhanced edge oxide thickening. From the discussion so far, no difference is expected to exist in edge oxide thickness and its LCI $V_g$ correlation between NMOS and PMOS devices. Further experiments have also been performed in order to correlate LCI $V_g$ with the MOSFET degradation under stress. Drain avalanche hot carrier stress causes degradation near the drain edge and is sensitive to plasma edge damage. Even if devices are processed under different conditions, it can be expected that devices with greater edge damage would exhibit higher hot carrier degradation. We should therefore expect a correlation between hot carrier degradation in devices on the ten wafers processed under different poly-Si etching conditions and the edge damage. Fig. 10 shows a correlation between hot carrier degradation in transconductance and LCI $V_g$ for PMOS transistors from the ten-wafer split. The wafers which show greater hot carrier degradation also have a larger LCI $V_g$. This is consistent with our hypothesis that enhanced edge damage leads to enhanced edge oxide thickening.

In order to establish the correlation between LCI $V_g$ and hot carrier degradation in individual devices across the wafer, two of the wafers from the ten-wafer split were chosen for more detailed reliability studies. Wafer A had less edge damage and wafer B had greater edge damage, as seen from Fig. 10. Hot carrier degradation and LCI $V_g$ were measured across both the wafers and the results are shown in Fig. 11. Each point in the figure is a measurement made on an indi-
individual PMOS transistor under the appropriate measurement conditions. There is a strong correlation between LCI $V_g$ and hot carrier degradation across the wafers and in both wafers A and B. Therefore, the excellent correlation found between ‘edge oxide thickening’ and device performance and reliability shows that both are affected by plasma edge damage, introduced during poly gate etch. To ensure that the effect of plasma damage induced thickening is a real process-induced effect and not an artifact observed in particular processing lots, the following experiment was done. Two wafers were processed identically except for poly-Si etching step which was performed in two different plasma tools. The results obtained are given in Table I and are consistent with previous experiments. Table I shows LCI $V_g$ for NMOS devices along with data from reliability tests such as FN stress, hot-carrier stress and LCI stress. LCI stress corresponds to the injection of carriers into the localized region near the gate edge for a specific duration. LCI $V_g$ for virgin devices is higher for Etcher X devices than for Etcher Y devices, indicating that Etcher X caused greater edge damage. All the stress results also indicate that Etcher X devices show a larger degradation when subjected to stress indicating greater edge damage. This clearly validates the LCI as a measurement tool for study of plasma induced edge damage in submicron MOSFET’s.

### IV. Conclusions

A simple and accurate electrical technique for characterization of plasma induced edge damage in submicron MOSFET’s is proposed. The application of this technique for a study of edge damage from split to split has been demonstrated and correlated with the device performance and reliability. This method therefore provides a sensitive measure of plasma etch damage on the MOSFET characteristics and reliability.

### REFERENCES


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