Application of Look-up Table Approach to High-K Gate Dielectric MOS Transistor circuits

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Abstract

In this paper, we study the circuit performance issues of high-K gate dielectric MOSFETs using the Look-up Table (LUT) approach. The LUT approach is implemented in a public-domain circuit simulator SEQUEL. We observed an excellent match between LUT simulator and mixed mode simulations using MEDICI. This work clearly demonstrates the predictive power of the new simulator, as it enables evaluation of circuits directly from device simulation results without going through model parameter extraction.

1. Introduction

Development of physics based circuit models for deep sub-micron MOSFETs is becoming increasingly difficult as the device dimensions are scaled down. Earlier, it had been possible to obtain compact models with a small number of fitting parameters for circuit simulation by understanding the physical phenomena in the devices. This is no longer practical as the device dimensions enter the sub 100 nm regime, since these devices have very complex structures and doping profiles. To model the small geometry devices accurately, one has to perform multidimensional analysis, which always results in very complicated model expressions with many empirical parameters. Further, it is generally difficult to extract such a large number of parameters accurately from experimental data, and parameters extracted often produce parameters which are physically inconsistent. Because of the above difficulties with analytic models, the look-up table (LUT) approach is being considered as an attractive alternative for circuit simulation [1, 2]. In this approach the terminal currents and charges are used as Look-up table. A suitable interpolation scheme is used to evaluate the current or charge at any point that does not coincide with a table point. In this paper, we will describe the application of the LUT approach to study the circuit performance of the high-K gate dielectric MOSFETs.

2. Look-up Table Method

In the LUT approach, our aim is to approximate the behaviour of a given device using finite number of table points with a suitable interpolation algorithm. The table points can be obtained from measurements, device simulations, or from existing physical models. In semiconductor device models, the controlling variables of the device are its terminal voltages and the dependent physical quantities are its terminal currents and charges. The objective is to approximate this dependent physical quantity using an interpolation scheme. It is assumed that the device operates in quasi-static regime [5], i.e., the terminal currents and charges depend only on the instantaneous values of the terminal voltages. As we shall see in Section 4, this assumption is a realistic one in many practical situations with sub-micron gate lengths.

3. Extraction of Look-up Table from device simulations

For MOSFETs, the terminal currents can be expressed as

\[
I_x(t) = I_X(V_{BS}(t), V_{GS}(t), V_{DS}(t)) + \frac{dQ_X(V_{BS}(t), V_{GS}(t), V_{DS}(t))}{dt}
\]

where X can be gate, drain, source, or substrate. \(I_X\) is the DC current that would result if the bias voltages were to be held constant at their instantaneous values. Similarly, \(Q_X\) is the terminal charge corresponding to the instantaneous values of the bias voltages. Note that, Eq. 1 does not explicitly include the “past history” of the device; in other
words all NQS effects are ignored. In the LUT method, the MOSFET is modeled as a table of DC currents $I_D$, $I_G$, $I_B$ and terminal charges $Q_B$, $Q_G$, $Q_D$ for the desired range of bias voltages, and the terminal currents are computed using Eq. 1 using a suitable interpolation scheme. The tables can be generated by experimental measurements or device simulation; as no approximations are made in generating the tables, the LUT model represents an “exact” QS model.

The current $I_X$ in Eq. 1 can be obtained by DC simulation for the required range of bias voltages. The charge denoted by $Q_X$ in Eq. 1 is much more subtle. It is not simply the terminal charge obtained with device simulator. To appreciate this point, consider particularly the bulk (or “body”) terminal of a MOS transistor. The device simulator will always produce a negligible value of $Q_B$ since the electric field in the neutral region near the bulk contact is very small, producing a small $Q_B = \int E \cdot dS$. So, the use of $Q_B$ computed by DC simulation for LUT quasi-static model, will always predict a vanishingly small $I_b(t)$, irrespective of bias voltages. This prediction is obviously incorrect: particularly when an applied voltage ramp takes the device from accumulation to inversion, a significant bulk current must flow. In order to extract the terminal charges accurately from device simulations, we have used the terminal charge extraction technique using transient simulations described in [3]. For generating the current and charge look-up tables for the examples discussed in this Section, we have used the ISE-TCAD [6] package. In extracting the terminal charges a gate ramp (from a low voltage to high voltage) with an appropriate rise time $\tau_r$ was applied; $\tau_r$ is chosen to be much larger than the transit time, thus ensuring that the device remains in the QS regime. It is instructive to look at an example of the terminal charge extraction. Fig. 1 shows the drain terminal transient current obtained using ISE-TCAD, and the corresponding terminal charge extracted from the transient current is shown in Fig. 2. In these simulations, a gate ramp going from -2 V to 5 V was applied, with $\tau_r=10$ nsec, and the simulated device had gate length of $L=2 \ \mu m$.

Having computed the terminal currents and charges for the device concerned at the “table points”, the next step is now to implement the look-up table approach in a circuit simulator. For this purpose, the SEQUEL circuit simulation program [7] was used, as it allows new device models to be easily incorporated. Interpolation between table points (“grid points”) was carried out using the techniques described in [1]. In the following, we will refer to this implementation simply as the LUT model.

The LUT model, as constructed using the above procedure, was validated by detailed comparison with device simulation results. Gate and drain voltage pulses with various values of rise and fall times were applied to the device for this purpose and it was verified that all transient currents obtained with ISE-TCAD and the LUT model matched per-
fectly. The rise and fall times of the applied $V_G$ and $V_D$ pulses were chosen such that the device remained in the QS regime.

4. Application to High-K Gate Dielectric MOS Transistor Circuits

It is well known that, as the gate length $L$ is scaled down, the oxide thickness must also be reduced in order to suppress the short-channel effects. For example, for $L=50$ nm, the oxide thickness needs to be as small as 0.8 nm [8]. With such a thin gate oxide, direct tunneling occurs, which will increase the power dissipation and will deteriorate the device performance and circuit stability [8, 9]. The use of high dielectric constant ("high-K") gate insulators has been proposed [4] to alleviate the gate leakage problem in sub 100 nm MOS transistors. With a high-K dielectric replacing the oxide, one can increase the insulator thickness by a factor of $K/K_{ox}$ and still obtain the desired gate capacitance. However, as studied recently, the device performance is known to degrade considerably due to the gate fringing fields, when a high-K dielectric material is employed [10, 11]. Although, the device performance with high-K gate dielectrics has been studied in detail [11], evaluation of circuit performance has not received much attention. This is due to the fact that accurate analytical models for high-K transistors are not yet developed which take into account the fringing field effects. The LUT model, on the other hand, does not require analytical device models and is therefore ideally suited for prediction of circuit performance with high-K transistors. For the LUT model, the device characteristics of the MOS transistors with different high-K gate dielectrics were extracted using two-dimensional device simulator MEDICI [12]. The simulated structures, which are based on scaled device dimensions outlined in the SIA road-map, have a gate length down to 70 nm and oxide thickness of 1.5 nm. A spacer technology with heavily doped source/drain extensions is used. The source/drain extension and deep source/drain junction depths are 30 nm and 50 nm respectively. The permittivity of the gate dielectric (K) is varied from 3.9 to 100 keeping the "effective" gate dielectric thickness constant at 1.5 nm. A calibrated energy balance model is incorporated to consider the spatial variation of carrier energy in order to account for the velocity overshoot and non-local transport phenomena. The Fermi-Dirac statistics is used for the active carrier density within the simulation structures.

Before applying the LUT approach to the high-K transistor circuits of interest, the LUT model was validated using the mixed-mode capability of MEDICI [12]. In particular, a CMOS inverter was simulated using both MEDICI and the LUT model with an input pulse ($\tau_r=\tau_f=10$ psec). The results are shown in Fig. 3, and an excellent match can be clearly seen between the MEDICI and LUT results. This shows that, for $\tau_r$ and $\tau_f$ as small as 10 psec, the LUT model accurately predicts the circuit performance. One of the important parameters to be considered in the CMOS circuit design is the propagation delay $t_p$ of the gate, as it defines how quickly the gate responds to a change in the input and relates directly to the speed and performance metrics. The ring oscillator is the standard circuit for delay measurement. The propagation delay $t_p$ can be obtained by measuring the time period ($T$) of oscillations and by using the formula $T = 2t_pN$, where $N$ is the number of inverters in the chain. We have simulated a 25-stage ring oscillator to measure the average inverter delay with different high-K gate dielectrics. Fig. 4 shows the inverter delay as a function of $K$. With increase in $K$, the parasitic capacitance decreases due to higher physical gate dielectric thickness (lines of forces has to travel more distance to reach source/drain regions from gate electrode) [13]. Thus, the frequency of oscillations increases with increase in $K$ value (see Fig. 5). Static-power dissipation is another important issue in circuit design. This is due to the leakage currents in the device. It is well established in the literature that the short channel performance degrades with increase in $K$ value which results in higher sub-threshold currents. To study the effect of sub-threshold leakage currents on the circuit performance, we have simulated dynamic gates. The operation of the dynamic gates relies on the dynamic storage of the output value of the capacitor. In the precharge phase (when $\phi=0$) the output node
Delay (pico sec)

$K_{eq} = 1.5 \text{ nm}$

$L = 70 \text{ nm}$

$\frac{(W)_p}{(W)_n} = 3.0$

Figure 4. Average inverter delay obtained by simulating a 25 stage ring oscillator for different values of $K$.

Figure 5. Output waveform of a 25-stage ring oscillator made-up of MOS transistors with gate dielectrics $K=3.9$ and $K=100$, obtained by LUT simulator.

Figure 6. Output voltage of a 2-input dynamic NAND gate with time for different high-K gate dielectrics.

is charged to Vdd and in the evaluation phase (when $\phi=1$) the output voltage is determined by the combination of inputs. Initially we precharged the output voltage of the 2-input dynamic NAND gate to Vdd and then kept the gate in evaluation phase for a long time with both inputs grounded. Ideally the output voltage should remain at logic 1. But due to leakage currents, this charge gradually leaks away resulting eventually in malfunctioning of the gate. As can be seen from the figure 6, with increase in the value of $K$, this problem becomes more severe. It can also be observed that in dynamic NOR gates this problem is more enhanced due to the parallel combination of the evaluation transistor (Fig. 7).

We have also simulated a domino logic gate with different high-K gate dielectric materials. The circuit shown in Fig.8 consists of a $\phi$ block followed by a static inverter. This ensures that all inputs to the next logic block are set to zero after the precharge period. Due to the sub-threshold leakage currents during evaluation period, $V_1$ starts to fall (discharges) even though $V_{in}$ (N1 is off) is held at logic 0 and this discharging is faster for a circuit where high-K dielectric is employed as a gate material. Thus, when $V_1$ reaches below the threshold voltage of the static inverter, its output ($V_2$) goes to logic 1. This results in $V_{out}$ being discharged to logic 0, which is not the correct state. Now with a higher K material, this state is reached faster due to the higher leakage currents (Fig. 9).
5. Conclusions

A Look-up table based circuit simulator has been presented in this work. We also presented the simulation of circuits with high-\( K \) gate dielectric MOSFETs and analyzed the performance of the circuits in terms of delay and leakage currents. It is observed that with increasing value of gate dielectric constant the speed of operation of devices increases but at the same time the sub-threshold performance degrades leading to higher leakage current and malfunctioning of dynamic circuits. The LUT simulator is therefore an attractive alternative for circuit simulations employing novel technologies, where analytical model development is often complicated and time consuming.

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References


