Optimizing MOSFET Channel Width for Low Phase Noise in LC Oscillators

Jayanta Mukherjee,
Assistant Professor
Department Of Electrical Engineering
Indian Institute of Technology, Bombay
Powai, Mumbai 400074, India
jayanta@ee.iitb.ac.in

Abstract — Phase Noise is an important consideration in oscillators. A procedure to obtain low phase noise through MOSFET channel width optimization is described in this paper. The impact of channel width is different for white and flicker noise. The Phase Model used for this purpose is based on a circuit based model. While the Phase Noise due to white noise increases with channel width increase, that due to flicker noise decreases, thereby setting up the conditions for optimization. We derive mathematically that optimum channel width that results in the lowest phase noise with other parameters remaining constant and verify our results by simulation.

I. INTRODUCTION
Phase Noise is an important design attribute in LC oscillators, especially at RF frequencies. It is defined as the spectral density of the oscillator voltage (or current) spectrum at an offset from the center frequency of the oscillator relative to the total power of the oscillator. In time domain it is more common to refer to this phenomenon as phase jitter. A perfect oscillator would have localized tones at discrete frequencies (i.e, harmonics) but any corrupting noise spreads these perfect tones, resulting in high power levels at neighboring frequencies. This effect is the major contributor to undesired phenomena such as inter-channel interference, leading to increased bit error rates (BER) in RF communication systems. Another manifestation of the same phenomenon, jitter, is important in clocked and sampled-data systems. Uncertainties in switching instants caused by noise lead to synchronization problems.

The modern wireless standards place strict restrictions on the noise that can be allowed. Various methods of phase noise optimization are present as described in [1], [2], [3]. In [1], the optimization involves system level design techniques, while in [2], the optimization is done using CAD tools. In [3] the optimization involves choosing the right combination of \( L \) and \( C \) which leads to lowest Phase Noise. In [4] it is shown that white noise increases with increase in width whereas the flicker noise is independent of the channel width with other parameters remaining constant. In this paper we show how MOSFET channel width optimization can be used to minimize phase noise. As we shall see in Section II, the oscillator phase noise due to flicker noise decreases with increase in width. For constant bias current the channel width acts differently on the phase noise due to white noise and that due to flicker noise. We analytically obtain the value of channel width that produces the minimum phase noise. We then verify our predictions by simulation on a differential oscillator. The simulation tool used is Agilent ADS.

II. PHASE NOISE EXPRESSION

An equivalent circuit diagram of an oscillator is given in Figure 1. \( Y_L \) and \( Y_{IN} \) represent the impedances of the tank part and that of the device part (consisting transistors) respectively. \( i_N \) is the equivalent noise current produced by both the device and the tank parts of the circuit. The general expressions for a circuit based phase noise expression due to white and flicker noise is given in [5] and [6]. The Phase Noise expression due to white noise is Lorentzian and given by [5],

\[
S_{F,\text{white}}(\omega) = \frac{A_0^2}{2} \left[ \frac{m_1}{m_1^2 + (\omega - \omega_k)^2} \right]^{1/2} \left[ 1 + \frac{c}{2} \left( \frac{m_1 + m_2}{(m_1 + m_2)^2 + (\omega - \omega_k)^2} \right) \right]^{1/2}
\]

The derivation of the above expression flows from a non linear perturbation model first developed by Kurokawa [9]. The expression for Phase Noise due to flicker noise is given by [6],
The above expression is obtained using a trap level model of flicker noise and by establishing an equivalence of perturbation in oscillation due to flicker noise and bias instability. The expressions above can be simplified as shown in [7] and the expression for the combined Phase Noise due to both white and flicker noise can be given for small offset frequencies as,

\[ L = \frac{S_{\text{inst}, \text{th}}}{A^2} \]

\[ = \frac{1}{P_S} \left[ i_{N, \text{white}}^2 \left( 1 + \cot \theta \right) \frac{\omega^2}{\Delta \omega^2} \right] + \frac{i_{N, \text{ff}}^2 \left( G_{\text{in}}^2 - B_{\text{in}}^2 \cot \theta \right)^2}{\Delta \omega^2} \]

(1)

Figure 1: A simplified oscillator circuit

Where, \( P_S = \frac{1}{2} A^2 g_L \cdot \theta \), as shown in Fig 2, is the angle between the locus of \( Y_{IN} \) on the z-plane with respect to the amplitude \( A \) of oscillation, and the locus of \( Y_L \) on the z plane with respect to frequency. \( Q \) represents the Q-factor of the tank and is given by, \( Q = \omega_0 \frac{\text{Im}(Y_L)}{2Q} = \omega_0 C / G_L \).

\( Y_{IN} = G_{IN} + jB_{IN} \) represents the derivative of the input admittance of the device with respect to dc bias current variation.

III. CHANNEL WIDTH OPTIMIZATION

Equation (1) can be used to find a lower bound on the Phase Noise wrt transistor channel width i.e. the best Phase Noise performance that can be achieved by modifying the transistor channel width. As we can see from Equation (1), with increasing bias stability the phase noise due to the flicker noise will reduce. This however is different from the process of flicker noise however as shown in [4] where the flicker noise is independent of channel width. Bias stability depends on transistor width, the higher the width, the lower is the deviation in admittance due to change in bias current. On the other hand, increase of width leads to higher white noise current.

Figure 2: Loci of \( Z_m \) and \( Z_L \) on the Z Plane. The point of intersection of the two loci corresponds to the operating point.

Hence there has to be a compromise in the width that a transistor can have so as to achieve the lowest possible phase noise. This is basically an optimization problem which we would like to quantify. The oscillator topology used, is the differential oscillator shown in Fig 2. The flicker noise current of a MOSFET is given by,

\[ i_{N, \text{ff}}(f) = C g_m^2 \]

(2)

where, \( C \) is a constant. When the dc bias current of the MOSFET is constant as is the case in the differential oscillator topology shown the transconductance \( g_m \) is given by,

\[ g_m^2 = 2 \mu C \frac{W}{L} I_d \]

(3)

From which the expression for flicker noise reduces to,

\[ i_{N, \text{ff}}(f) = \frac{2 \mu K J_d}{L^2} \]

(4)

This clearly shows that the flicker noise current is independent of width of the transistor for constant bias. On the other hand due to the dependence of the bias derivatives terms \( G_{IN} \) and \( B_{IN} \) on \( W \), the Phase Noise due to flicker noise current reduces by a factor \( W^p \) (p ranging between 1 and 2)
for the same flicker noise current. This can be stated as, 

\[ G_{\text{IN}}^{\nu} - \cot(\theta)B_{\text{IN}}^{\nu} = \frac{K}{W} \]

where, \( K \) is a constant. This result was observed through simulation. Further, the white noise current of a MOSFET is given by,

\[ i_{\text{white}}^{\nu}(f) = \frac{8}{3}kTg_{m} = \frac{8}{3}kT\sqrt{2\mu C_{ox} W}{L} I_{d} \]  

(5)

which shows that the white noise current increases by a factor \( \sqrt{W} \) for increasing \( W \). A similar result is obtained if short channel effects are also considered. Hence the total Phase Noise can be written as,

\[ PN = N\sqrt{W} + \frac{R}{W} \]

(6)

where,

\[ N = \frac{2}{3}kTQ^{2}P_{s}\sqrt{\left(1 + \cot^{2}(\theta)\right) \frac{\omega^{2}}{\Delta \omega}} \]

\[ R = \frac{\mu C_{L} K \omega_{0}^{2}}{2L^{2}Q^{2}G_{C}^{2}f_{\Delta \omega}^{2}} \]

The minimum value of Phase Noise is obtained by taking,

\[ \frac{d(PN)}{dW} = 0 \quad \text{which gives,} \]

\[ W_{\text{min}} = (\frac{2R}{N})^{\frac{1}{2}} \]  

(7)

It can be shown that \( W_{\text{min}} \) is indeed a minima because,

\[ \frac{d^{2}(PN)}{dW^{2}}(W = W_{\text{min}}) \geq 0 \quad \text{for all } W. \]

IV. DIFFERENTIAL OSCILLATOR CIRCUIT ANALYSIS

In the equations derived in the previous sections we had mentioned the equivalent noise current \( i_{\nu} \). Reference [8] illustrates the method used for the differential oscillator analysis. The noise currents of the individual transistors are analyzed into four non-correlated modes as shown in Fig 5.

Let \( |i_{1}|^{2} = |i_{2}|^{2} = a \) and \( |i_{+}|^{2} = |i_{-}|^{2} = b \), \( a \) and \( b \) being the power densities of the PMOS and NMOS transistor noise currents respectively. In Fig5 \( \mu, \nu \) and \( \gamma \) are given by,

\[ \mu = \sqrt{\frac{ab}{2(a+b)}}, \nu = \frac{a}{\sqrt{2(a+b)}}, \gamma = \frac{b}{\sqrt{2(a+b)}} \]

Intuitively from Fig 5, we can deduce that Modes A and C play the most significant role for Phase Noise due to flicker noise. This is because, in Mode A noise currents \( 2\mu \) enter the oscillator core both at the top and the bottom. Flicker noise manifests itself as Phase Noise by the process of upconversion of noise. When the noise currents \( 2\mu \) enter the oscillator core in Mode A, due to the alternate switching of the NMOS and the PMOS transistors, a mixer like action takes place because of which the flicker noise at dc is upconverted to the RF frequencies. This way flicker noise at dc appears as Phase Noise at RF frequencies. Similarly for Mode C, the noise currents entering the oscillator core at the top and bottom are \( 2\nu \) and \( 2\gamma \) respectively. For Modes B and D the noise currents entering the oscillator core both at the top and at the bottom are zero. Thus there is no upconversion of noise taking place for these modes. Hence the Phase Noise produced by these modes at RF is primarily due to the white noise present at the same frequencies. Further details of mathematical derivations and simulation results are given in [8]. It can be shown that the equivalent noise current \( i_{\nu} \) for both white noise and flicker noise is given by [8],

\[ |i_{\nu}|^{2} = 4\mu^{2} + (\nu - \gamma)^{2} = \frac{a + b}{2} \]  

(8)

V. SIMULATION RESULTS

The circuit used for simulation is the differential oscillator shown in Fig 3. For simplicity only noisy PMOS transistors were used and the corresponding change in impedance was noted. The NMOS transistor noise was turned off. \( Y_{IN}' \) is computed by injecting a signal at the frequency of oscillation at various amplitudes of oscillation, into the nonlinear part of the oscillator and noting the change of input admittance. \( Y_{IN}' \) is computed similarly by finding the change of admittance for various values of dc current bias change. Reference [7] gives the details of these derivations.

The equivalent noise current due to the 2 noisy transistors was obtained using the analysis technique presented in section IV. Plugging the values into equation (7) gives the value of \( W_{\text{min}} = 2.16 \mu \). Here \( W_{\text{min}} \) refers to the optimized width of both the PMOS transistors. This is indeed what is actually observed in simulation as shown in Fig 3. For either \( W = 5 \mu \) or \( W = 1 \mu \), the phase noise obtained is higher that obtained for \( W = 2 \mu \) (close to the minima).

One aspect of oscillator design we haven’t mentioned so far is that whatever optimization scheme we employ, it must satisfy the basic oscillation criterion for negative resistance oscillators. The criterion can be given as,

\[ Y_{IN}(\omega_{0}, A_{0}) = -Y_{L}(\omega_{0}, A_{0}) \]

(9)

So the optimized width obtained from Equation (7) must also satisfy the requirements of Eqn (9). For \( W = 3 \mu \) or \( W = 4 \mu \), the above requirements were not satisfied and no oscillation was obtained. As a result the corresponding Phase Noise graphs for these channel widths are not shown in Fig 4.
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REFERENCES

Figure 3: A differential oscillator showing the equivalent current noise sources of the transistors

Figure 4: Comparison of Phase Noise obtained at various values of W. At W=2um the lowest Phase Noise is obtained for a frequency offset of 100 KHz

Figure 5: Differential oscillator modes