Stress Voltage Polarity Dependence of JVD-Si$_3$N$_4$ MNSFET Degradation

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Abstract—In this paper, we study the stress voltage polarity-dependent reliability of n-channel metal-nitride-silicon field-effect transistors (MNSFETs) with ultrathin jet vapor deposited (JVD) silicon nitride dielectric. Under constant voltage stress, device parameters such as threshold voltage and transconductance degrade. Charge trapping due to interface and bulk traps is observed. Our study shows that the degradation is polarity dependent. MNSFETs show lower degradation under positive stress fields. We have also compared the performance of MNSFETs with conventional MOSFETs under identical stress conditions. Under positive stressing, MNSFETs clearly outperform MOSFETs, but under negative stressing, MNSFETs show more degradation.

Index Terms—High-field stressing, high-κ, MNSFETs, polarity dependence.

I. INTRODUCTION

ALTERNATIVE high-κ dielectrics are needed to replace conventional SiO$_2$ in MOS transistors to reduce the gate leakage currents. Many materials have been investigated for possible replacements to SiO$_2$. Silicon nitride is one such dielectric, which has dielectric constant of 7.5, approximately twice that of SiO$_2$. Its imperviance to boron, sodium, and moisture is well known. Although traditional chemical-vapor-deposition (CVD) deposited nitrides had lots of traps, recently with jet vapor deposition (JVD), excellent quality films have been obtained [1]. With current scaling trends, JVD Si$_3$N$_4$ can be used at least up to the 100-nm node. Beyond this, other high-κ materials with higher k values will be needed. Some of the materials with high-κ values are hafnium and zirconium oxides and silicates. JVD MNSFETs have shown promise as alternative dielectric with improved hot-carrier performance compared to conventional MOSFETs [2]. However, reliability under high-field stress is not known. Conventional MOSFETs with ultrathin SiO$_2$ gate dielectric have shown increased interface generation under high-field stressing causing $V_{th}$ and $g_m$ degradation. In MOSFETs, the degradation and hence $Q_{BD}$ is known to be polarity dependent [3]–[8]. In this paper, we study the polarity-dependent reliability of n-channel MNSFETs and compare performance of MNSFETs with MOSFETs under equivalent stress conditions.

II. DEVICES

Devices used in this study are n-channel n$^+$ poly-Si gate transistors. These were fabricated using an identical CMOS process except the gate deposition process. One set of transistors has Si$_3$N$_4$ as the gate dielectric deposited using the JVD process [1] followed by annealing in 800°C for 25 min in N$_2$ (henceforth referred as MNSFETs). The second set of transistors have SiO$_2$ grown at 800°C followed by an in-situ anneal in N$_2$ (henceforth referred as MOSFETs). The MNSFETs have an equivalent oxide thickness (EOT) of 3.1 nm and the MOSFETs have gate-oxide thickness of 3.9 nm. The transistors have $W \times L = 10 \times 0.18 \mu$m$^2$.

III. EXPERIMENT

The transistors were subjected to high-field stressing with constant voltage applied to the gate with the source, drain, and substrate grounded. The stress was interrupted periodically to monitor the changes in the gate threshold voltage $V_{th}$, transconductance $g_{max}$, and $N_{it}$. The values of $V_{th}$ and $g_{max}$ were obtained from the $I_D$–$V_{GS}$ characteristics measured at a drain bias of 50 mV. The peak transconductance was calculated from the $I_D$–$V_{GS}$ data. Charge pumping current was measured by applying a trapezoidal waveform of 1-MHz frequency to the gate with a rise and fall time of 250 ns. $N_{it}$ was calculated from the charge pumping current.

IV. RESULTS

Pre-stress characteristics of MNSFETs and MOSFETs: The pre-stress $I_D$–$V_{GS}$, $g_m$–$V_{GS}$, and charge pumping characteristics of an MNSFET and MOSFET are compared first. The pre-stress $I_D$–$V_{GS}$ and $g_m$–$V_{GS}$ characteristics of the transistors are shown in Fig. 1. Both $I_D$ and $g_{max}$ are normalized with $C_{ox}$. The normalization is required since the EOTs and hence the gate capacitances are slightly different for MNSFETs and MOSFETs. The threshold voltages ($V_{th}$) of MOSFET and MNSFET obtained from the maximum slope of $I_D$–$V_{GS}$ characteristics are 0.43 and 0.47 V, respectively. The pre-stress transconductance $g_m$ of MOSFETs is comparable to that of MNSFETs. The pre-stress $I_{CP}$ is plotted in Fig. 2 for MOSFET and MNSFET. The average pre-stress $N_{it}$ is of the order of $1 \times 10^{10}$ cm$^2$ in MOSFETs and about $4 \times 10^{10}$ cm$^2$ in MNSFETs. MOSFETs and MNSFETs have comparable pre-stress characteristics except for the interface state density $N_{it}$ that is slightly higher in the case of MNSFETs. This is expected since the Si/Si$_3$N$_4$ interface has more traps compared to the Si/SiO$_2$ interface.

Post-stress performance of MNSFETs and MOSFETs: MNSFETs and conventional MOSFETs were subjected to constant voltage stress. The gate voltages applied are scaled according to the $V_{th}$. The fields are kept constant at +12 and +14 kV/cm as well as −11 and −12 MV/cm. The effect of stress on transconductance ($g_{max}$) and threshold voltage ($V_{th}$) is studied.
Fig. 1. Pre-stress $I_D-V_{GS}$ and $g_{max}$ characteristics of MNSFET and MOSFET.

Fig. 2. Pre-stress $I_D-V_{GS}$ characteristics of MNSFET and MOSFET.

Fig. 3. Comparison of effect of positive stress fields on $g_m$ in MOSFETs and JVD MNSFETs. $\Delta g_m = |g_{max} - g_{max,0}|$ is plotted as a function of time.

Fig. 4. Comparison of effect of negative stress fields on $g_m$ in MOSFETs and JVD MNSFETs. $\Delta g_m = |g_{max} - g_{max,0}|$ is plotted as a function of time.

A. Evolution of $g_{max}$

$\Delta g_m$, which is defined as $|g_{max} - g_{max,0}|$ for positive stressing, is shown in Fig. 3. The most important result, which we can see, is that peak transconductance degrades much more slowly in nitrides than oxides. It is clear that for positive fields, MNSFETs show better performance compared to MOSFETs. Next, we compare the performance of MNSFETs with MOSFETs under negative stress fields equal to $-11$ and $-12$ MV/cm. $\Delta g_{max}$ as a function of time is plotted in Fig. 4.

We can see that the $g_{max}$ degradation under negative stress is higher in both MNSFETs and MOSFETs compared to positive stress, but the degradation is lower in MNSFETs. Hence, under both positive and negative stress, $g_{max}$ performance is better in MNSFETs.

B. Evolution of $V_{th}$

We now look at the effect of positive and negative gate voltage stressing on threshold voltage. $\Delta V_{th}$, the change in threshold voltage, is defined as $(V_{th} - V_{th,0})$ where $V_{th,0}$ is the threshold voltage before stress. Both interface states and bulk trapping contribute to the variation in the threshold voltage. Therefore, we have separated the two contributions by subtracting the threshold voltage shift due to interface states ($\Delta V_{int}$) as follows:

$$\Delta V_{th} = \Delta V_{int}$$

(1)
Fig. 5. Effect of positive stress fields on $\Delta V_{it}$ in conventional MOSFETs and JVD MNSFETs plotted as a function of time.

Fig. 6. Effect of positive stress fields on $V_{it}$ in conventional MOSFETs and JVD MNSFETs plotted as a function of time.

where $\Delta V_{it}$ is voltage shift due to $\Delta N_{it}$, calculated as follows:

$$\Delta V_{it} = \frac{q\Delta N_{it}}{C_{ox}}.$$  \hspace{1cm} (2)

Here, $\Delta N_{it}$ is calculated as $(N_{it} - N_{it,0})$ where $N_{it,0}$ is the initial (pre-stress) interface state density and $N_{it}$ is the interface state density after stress. $N_{it}$ is calculated from the charge pumping currents. For positive stress, $\Delta V_{it}$ and $\Delta V_{it}$ are plotted in Fig. 5 and Fig. 6, respectively. $\Delta V_{it}$ shows a power-law dependence with stress time for both MNSFETs as well as MOSFETs. MNSFETs show lower shifts compared to MOSFETs. Hence, MNSFETs outperform MOSFETs under positive stress.

For negative stress, $\Delta V_{it}$ and $\Delta V_{it}$ are plotted in Fig. 7 and Fig. 8, respectively. We can see that the voltage shifts are higher in JVD MNSFETs, which show net negative trapping, whereas MOSFETs show positive bulk trapping. JVD MNSFETs do not outperform MOSFETs under gate negative stress.

Next, we look at the polarity dependence of stress in MNSFETs under a fixed field of 12 MV/cm.

C. Stress Voltage Polarity Dependence of MNSFETs

The stress voltage polarity-dependence in MNSFETs is studied for effective fields of 12 MV/cm and -12 MV/cm, respectively. The $I_D-V_{GS}$ characteristics and the charge pumping current $I_{cp}$ are illustrated in Figs. 9–12. The $I_D-V_{GS}$ characteristics shown in Fig. 9 and Fig. 10 show very little shift under positive stress as compared to negative stress. The
charge pumping current $I_{CP}$ is plotted in Fig. 11 and Fig. 12, respectively. The charge pumping current for positive stress is lower than that for negative stress by a factor of 4.

The normalized increase in $N_{dt}$ defined as $(N_{dt} - N_{dt,0})/N_{dt,0}$, transconductance $(g_{max} - g_{max,0})/g_{max,0}$, and threshold voltage $(V_{th} - V_{th,0})/V_{th,0}$ are plotted as a function of stress time in Fig. 13. We can see that compared to gate positive stressing, gate negative stressing produces higher $N_{dt}$, $g_{max}$, and $V_{th}$ shifts. The polarity dependence in MNSFETs is clearly seen from Fig. 13. We discuss the results in Section V.

V. DISCUSSION

As illustrated in Figs. 3 and 4, with varying stress time, $\Delta g_{max}$ shows power law ($\propto t^n$) dependence for both MNSFETs and MOSFETs for both positive and negative stress. For positive stress (inversion), the exponent value $n$ for $\Delta g_{max}$ in MNSFETs varies between 0.3–0.4. These values are similar to the value (0.3) observed in P-MNSFETs subjected to constant voltage Fowler–Nordheim stress under inversion [9]. We can see that both the magnitude and rate of degradation is smaller for MNSFETs for positive stress. In the case of MOSFETs, values of $n$ are about 0.4–0.46. Compared to MOSFETs, MNSFETs show lower magnitude and slightly lower values of $n$.  

Fig. 9. $I_F-V_{GS}$ plotted as a function of stress time for a JVD MNSFET stressed at $E = +12$ MV/cm.

Fig. 10. $V_{GS}$ plotted as a function of stress time for a JVD MNSFET stressed at $E = -12$ MV/cm.

Fig. 11. $I_{CP}$ plotted as a function of stress time for a JVD MNSFET stressed at $E = +12$ MV/cm.

Fig. 12. $I_{CP}$ plotted as a function of stress time for a JVD MNSFET stressed at $E = -12$ MV/cm.
Polarity-dependent degradation in MNSFETs is clearly visible in Fig. 13. In the case of MOSFETs also, we see that the damage due to negative stress is higher compared to the positive stress. Polarity-dependent degradation in ultrathin MOSFETs is well known. It is attributed to the presence of defects at the gate/dielectric interface [4], the presence of a structural transition layer at the substrate/dielectric interface [5], or the difference in the electron energy dissipated at the anode which in turn depends on the anode Fermi level [6], [7]. According to this Fermi-level dependent anode hole injection (AHI) model, damage is maximum for p-type anodes where the electron impact generates hot holes. The defect generation rate is higher when the density of holes is larger in the anode [8]. We have used the Fermi-level-dependent AHI model as one of the possible mechanisms to explain the polarity-dependent degradation in MNSFETs. The band diagram of MNSFET in accumulation and inversion is shown in Fig. 14.

MNSFETs show lesser $\Delta g_{hn}$ and $\Delta V_{th}$ degradation than MOSFETs under positive stressing. This may be due to the higher bond breaking energy of Si–N bonds. However, under negative stress $\Delta V_{th}$ is higher than oxides which may be due to the increased hot-hole flux due to the smaller hole barrier height in nitrides (1.9 eV as compared to 4.9 eV). If an electron arrives with an energy of 3 eV, it impact ionizes to create a hole with a maximum energy of $3 - 1.1 = 1.9$ eV, which is comparable to the $Si_3N_4$/Si barrier of 1.9 eV. Compared to this, hole flux in SiO$_2$/Si would be smaller where the barrier height for holes is 4.9 eV.

VI. CONCLUSION

MNSFETs perform better compared to MOSFETs under positive bias, which is important for n-channel devices. The transconductance degradation is lower compared to MOSFETs. Also, there is no bulk trap generation in MNSFETs and, hence, threshold voltage shifts are also smaller. We can, therefore, conclude that the JVD MNSFETs can easily outperform MOSFETs under gate positive condition, that is, when the transistor is in inversion. However, the degradation of threshold voltage in MNSFETs is larger compared to MOSFETs under negative stress fields, that is, when the surface is in accumulation, although transconductance degradation is lower. By controlling the initial bulk trap density, JVD MNSFETs can be expected to outperform MOSFETs. Scaling $Si_3N_4$ down to 1.4 nm where the physical thickness is about 2.8 nm still shows charge trapping [9]. So, controlling the initial bulk trap density is the only way to reduce charge trapping. This can only be done by careful control of processing conditions. In the case of MNSFETs, it is known that water vapor annealing after deposition reduces bulk traps [10]. Hence, such techniques need to be explored in greater detail.

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REFERENCES


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