Abstract—CoolMOS™ is a novel power MOSFET with a “superjunction” for its drift region, which results in a vastly improved relationship between the on resistance and breakdown voltage. The presence of the superjunction makes the device physics very interesting and complicated. In this paper, we present simulation results aimed at understanding the device operation both in the on state and in the off state. Quasi saturation of the drain current is analyzed, and it is shown that it can be prevented by increasing the doping density of the drift region. An analytic model of the JFET-like drift region is presented. A CoolMOS™ transistor model based on the simulation results described here will be presented in an accompanying paper.

Index Terms—Device simulation, power MOSFET, superjunction.

I. INTRODUCTION

POWER MOSFETs are commonly used as switches in power electronic circuits; they should have minimal resistance ($R_{on}$) when the device is conducting and should sustain high voltages when the device is off. For a higher breakdown voltage ($V_{BD}$), power MOSFETs are commonly fabricated as a vertical double-diffused structure with a lightly doped “drift” epi layer to sustain the voltage. The breakdown voltage of the device is increased by reducing the doping concentration and increasing the thickness of this drift layer. However, this results in an increase in the on resistance. It can be shown that $R_{on}$ is proportional to $V_{BD}^2$ [1], which means that increasing $V_{BD}$ can result in a significant increase in $R_{on}$, causing higher conduction losses.

CoolMOS™ is a novel power MOSFET [Fig. 1(a)] projected as the latest milestone in high-voltage MOS devices [2]. In the CoolMOS™ device, the drift region of the conventional power MOSFET is replaced by a “superjunction,” i.e., a combination of n− and p− strips in parallel [2], [3] as shown in Fig. 1(a). When the device is on, the n− strip conducts the drain current. When the device is off, and a drain voltage $V_D$ is applied, it appears as a reverse bias between the n− and p− strips. A depletion region forms, and a relatively small value of $V_D$ fully depletes the drift region. Subsequently, the drift region behavior is similar to that of an intrinsic layer.

The behavior of the superjunction has been theoretically examined in detail earlier [4]–[8]. In this paper, we present device simulation results for CoolMOS™ and discuss the various physical phenomena in the off state and in the on state. In Section II, we analyze CoolMOS™ in the off state and explain its superior breakdown voltage as compared to a conventional power MOSFET. In Section III, the device behavior in the on state is presented, particularly, quasi-saturation of the drain current is examined in detail, and its cause is identified. An analytic model for the drift “pillar” is presented in Section IV.

II. COOLMOS™ TRANSISTOR IN THE OFF STATE

The behavior of the CoolMOS™ transistor in the off state is dominated by the characteristics of the superjunction drift layer. Analytic treatment of the superjunction under reverse bias has been given in [5]. Here, we will first explain, with the help of simulation results, why the breakdown voltage is higher in the superjunction structure. We will then discuss how the doping density of the n− and p− strips can be chosen to achieve the minimum on resistance.

A. Superjunction Versus Conventional Drift Layer

To understand how the superjunction drift region improves the breakdown voltage in the CoolMOS™ transistor, we simulate here the superjunction (SJ) alone (i.e., without the MOS transistor) and compare it with the drift region of a conventional power MOSFET, which is simply a lightly doped (LD) layer without any p-n junction. Fig. 1(b) shows the two simulated structures. The n+ and p+ contact regions are heavily doped ($N_d = N_a = 3 \times 10^{19} \text{cm}^{-3}$), the n− and p− strips, and the n− layer of the LD structure are lightly doped ($N_d = N_a = 3 \times 10^{15} \text{cm}^{-3}$). The p+ contact is grounded, and a positive voltage is applied to the n+ contact. The superjunction structure was found to break down at 300 V, while the LD structure could sustain only 130 V.

In Fig. 2(a), we have plotted the electric field for the LD structure. As this is effectively a one-dimensional (1-D) structure, there is no variation in the x direction. In Fig. 2(b), the net electric field for the SJ structure along the outer edge of the n− strip (see Fig. 1) is plotted. This field is also vertical because of symmetry. For the LD structure, the field profile is triangular, with constant slope, and advancing toward the n+ contact, as the applied voltage increases. Note that, in this structure, the depletion region expands gradually as the voltage increases. For the SJ structure, on the other hand, the n− and p− strips become completely depleted (which is indicated by the field becoming nonzero) at a relatively low voltage, about 50 V for this example. The field profile for larger voltages retains its relatively flat shape, with steep variations only near the contacts.
The following two observations, along with the field profiles, will explain the superior $V_B$ of the SJ structure: i) The voltage difference between the contacts in both LD and SJ structures is simply the area under the field profiles plotted in Fig. 2. This is because the electric field is vertical in both the structures, as we have pointed out. ii) It has been shown in [5] that, for the SJ structure, the field is maximum at the junctions along the two edges (and these two values are equal in our device because of symmetry). Thus, in each of the two structures, LD and SJ, the breakdown voltage is simply the area under the field profile when the maximum field reaches a critical value. Now, looking at the shape of the field profiles, it is easy to see that $V_B$ will always be higher for the SJ structure than that for the LD structure, because the area is larger in the SJ case.

When the height of the superjunction region (i.e., the n- and p- strips) was increased from 15 $\mu$m to 25 $\mu$m, without changing any other parameter, $V_B$ increased from 300 to 500 V. The field profiles at breakdown for the SJ structure for these two heights are seen to coincide almost exactly (Fig. 3) for 15 $\mu$m. Since $R_{\text{on}}$ has also increased in the same proportion as the height of the SJ region, the linear relationship between $R_{\text{on}}$ and $V_B$ for the SJ structure has been proved by this result.

In the SJ structures described so far, the doping density was not “optimized.” Using the analysis in [5], it can be shown that, for a given breakdown voltage $V_B$, there is an optimum doping concentration $N_0$ that results in the minimum on resistance (we have assumed the n- and p- strips to have the same doping density). $N_0$ is given by $N_0 \approx \varepsilon_s E_C/(0.742q_b)$, where $b$ is the width of each strip, and $E_C$ is the critical field. If $E_C$ is assumed to be constant for silicon, then there is a constant value of $N_0$ which gives minimum resistance of the drift region. The key observation is that $N_0$ is independent of the breakdown
Fig. 3. Electric field profiles along the right edge of the device [Fig. 1(b)] at breakdown, for SJ structures of heights 15 \( \mu \)m and 25 \( \mu \)m.

Fig. 4. Electric field profiles along the right edge of the device [Fig. 1(b)] at breakdown, for SJ structures with optimum doping density \( N_0 = 1 \times 10^{16} \) cm\(^{-3}\) and heights 15 \( \mu \)m and 25 \( \mu \)m.

Fig. 5. Depletion region edge in the CoolMOS™ device in the off state (\( V_{GS} = 0 \) V) for \( V_{DS} = 0, 3, 10, 20, 40, \) and 80 V. The axes correspond to those shown in Fig. 1(a).

Fig. 6. Transfer characteristics of the CoolMOS™ transistor [Fig. 1(a)] for various values of \( V_{DS} \).

B. CoolMOS™ in the Off State

The off-state behavior of the CoolMOS™ transistor can be expected to be very similar to that of the SJ structure described earlier. However, because of the MOSFET part, the CoolMOS™ structure is not symmetric. To see whether the breakdown voltage will be affected by the MOSFET part of the device, we simulated the structure shown in Fig. 1(a) with PISCES, and found \( V_B \) to be 317 V, which is marginally different than that in the SJ structure (300 V). Thus, the presence of the MOSFET part of the CoolMOS™ device does not change the breakdown voltage appreciably. We also found that the maximum electric field in the CoolMOS™ device and in the SJ structure are not very different.

In Fig. 5, the boundary of the depletion region in CoolMOS™ is shown for various applied voltages in the off state. It is seen that the drift region gets completely depleted at about 40 V of reverse bias.

III. On-State Simulations and Quasi-Saturation

In the on state, electrons flow from the source, under the gate electrode (i.e., through the MOSFET channel), through the drift region (i.e., the \( n^- \) part of the superjunction), to the drain terminal [see Fig. 1(a)]. We can therefore consider the device to be made up of an “intrinsic” MOSFET and a drift region. We have simulated the device in the on state, by applying a positive bias to the gate. The transfer characteristics (see Fig. 6) are similar to those of a conventional power MOSFET. The device turns on at the threshold voltage of the “intrinsic” MOSFET (about 6.9 V), and the current rises with \( V_G \) initially and saturates when the resistance of the drift region starts dominating. The characteristics saturate after a small increase in \( V_G \) (less than 1 V) in the simulated device, indicating a high drift region resistance, as compared to that of the intrinsic MOSFET. Note that in Fig. 6...
Fig. 7. Output characteristics of the CoolMOS™ transistor [Fig. 1(a)].

Fig. 8. Potential along the horizontal segment $y = 0 \mu m$ for the CoolMOS™ transistor [Fig. 1(a)] for $V_D = 25 V$ for various values of $V_G$.

Fig. 9. Depletion region edge in the CoolMOS™ transistor [Fig. 1(a)] in the on state ($V_G = 8.5 V$) for $V_D = 1, 5, 10, 15, 20, 25, 35, 50$, and $80 V$. The axes correspond to those shown in Fig. 1(a).

A. Observations Related to Quasi-Saturation

The quasi-saturation described earlier was thought to be due to degradation of mobility, as the electric field increases. To test the validity of this conjecture, the device was simulated with a constant mobility, and it was found that saturation indeed ceases to occur in this condition. This confirms that quasi saturation is related to mobility degradation. For a better understanding of quasi saturation, we have plotted, in Fig. 9, the depletion region edge for various values of $V_D$ and a fixed $V_G$ of 8.5 V. The depletion region is seen to be advancing on either side of the junction with increasing $V_D$. At about 10 V, at the “neck” (see the top right region of the figure) between the adjacent $p$ diffusions, the depletion region stops advancing into the $n^-$ side. This phenomenon is also seen at the lower part of the $n^+$ drift region (the “pillar” region) at about $V_D = 25 V$. Above this voltage, the depletion region edge remains stationary on the $n^+$ side and advances only on the $p^+$ side, as $V_D$ is increased.

The potential contours in the device at $V_D = 10 V$ (Fig. 10), for which quasi-saturation is beginning to occur, show that the highest field in the drift region occurs in the neck region. Hence, mobility degradation (due to velocity saturation) takes place in this region initially. This causes the differential resistance of this region to be large, and the additional voltage drop caused by an increase in $V_D$ would take place across this region. However, the potential profiles in the drift region for $V_D$ above 25 V showed that the additional drop distributes evenly throughout the drift region. This indicates that velocity saturation does begin to occur in the neck region first. But as $V_D$ is increased, eventually the entire drift region experiences high enough fields, leading to velocity saturation in the pillar region as well. This is to be contrasted with the conventional VDMOS transistor, in which velocity saturation occurs only in the neck of the drift region.

Once the electron velocity has saturated, further advancement of the depletion region (as $V_D$ is increased) would cause a decrease in the current, if the electron concentration is assumed...
observed that velocity saturation occurred in the drift region. As the intrinsic MOSFET is in saturation, this does not reflect on the $I_D-V_D$ curve.

### B. Supporting Increasing Bias After Quasi-Saturation

As we have seen above, the depletion region on the $n^-$ side of the drift region stops advancing when velocity saturation sets in, and the width of the depletion region in the $n^-$ pillar remains nearly constant over any subsequent increase in $V_D$. The question that arises now is: where is the additional drain voltage appearing, if the depletion region does not expand any further? Field profiles in the depletion region obtained from PISCES provide an explanation. It was inferred that the behavior of the potentials and fields in the quasi-saturated device is similar to that in the off-state device with a fully depleted drift layer. This is shown in Fig. 12(a) and (b); we can see that the shape of the field profiles in the depleted portion of the drift region remains constant after quasi saturation, only moving up with increasing $V_D$.

As quasi-saturation is a degrading effect, we need to either avoid it altogether in practice or make sure that it occurs at relatively large values of $V_G$. The earlier discussion of quasi-saturation suggests that this could be achieved by increasing the doping density of the $n^-$ and $p^-$ regions, which will stop the depletion region from advancing rapidly into the $n^-$ region. Accordingly, we increased the doping density from $N_d = N_a = 3 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$, which also happens to be the optimum doping density ($N_0$ of Section II) for this device. The new output characteristics (see Fig. 13) show quasi-saturation only above $V_G = 10 \text{ V}$. The more gradual spreading of the depletion region in this device as compared to the earlier structure can be clearly seen by comparing Figs. 9 and 14.

### IV. ANALYTICAL MODELING OF THE DRIFT PILLAR

The “pillar” portion of the $n^-$ drift region of the CoolMOS™ transistor is not present in conventional power MOSFETs, as we pointed out in Section III. Analytical modeling of this region was therefore undertaken, considering it to be equivalent to the JFET-type structure shown in Fig. 15, as suggested by the observed depletion region behavior. The gate, source, and drain terminals are defined for this JFET as shown in Fig. 15. Using the depletion approximation, we can write, assuming $N_a = N_d = N$

$$w(y) = \left( \frac{\varepsilon_s V_G}{qN} \right)^{1/2},$$

The total current at a given $y$ is

$$I = -\frac{zh(y)}{\rho} \frac{dV}{dy}$$

where $h(y) = a - w(y)$ ($a$ being the width of the $n^-$ pillar) can be shown to be

$$h(y) = a \left[ 1 - \left( \frac{V(y) - V_G}{V_p} \right)^{1/2} \right].$$
Fig. 12. Net electric field along vertical \((x = 4 \, \mu m)\) and horizontal \((y = 15 \, \mu m)\) segments for the CoolMOS™ transistor [Fig. 1(a)] with \(V_D = 8.5 \, V\) and different values of \(V_D\).

Fig. 13. Output characteristics of CoolMOS™ with \(N_d = N_a = 1 \times 10^{16} \, \text{cm}^{-3}\), device geometry being the same as that in [Fig. 1(a)].

Fig. 14. Depletion region edge in the CoolMOS™ transistor [Fig. 1(a)] with \(N_d = N_a = 1 \times 10^{16} \, \text{cm}^{-3}\) in the on state \((V_D = 8.5 \, V)\) for \(V_D = 1, 5, 10, 15, 25, 35, \) and \(50 \, V\). The axes correspond to those shown in Fig. 1(a).

Fig. 15. Structure identical to the pillar region, used for analytical modeling.

\(V_p\) in (3) is the pinch-off voltage \(V_p = q\alpha^2 N/c_s\). Now, integrating over the length of the structure, the current can be obtained as

\[
I = \frac{G_0}{2} V_D \left[ \frac{V_{DS}}{V_p} + \frac{2}{3} \left( \frac{-V_{GS}}{V_p} \right)^{3/2} - \frac{2}{3} \left( \frac{V_D - V_G}{V_p} \right)^{3/2} \right] \tag{4}
\]

with \(G_0 = 2\alpha^2/\rho L\). It can be seen that (4) is similar to that for a conventional JFET, except for a factor of half in the conductance and a factor of two in the pinch-off voltage.

For testing this model, a structure identical to the CoolMOS™ drift region was simulated with PISCES. As we have assumed in the derivation of (4) that there is no velocity saturation, a constant mobility was used for simulation. This assumption is realistic, because, as mentioned earlier, velocity saturation in the pillar region is a degrading effect which would be negligible in a properly designed practical device. The current–voltage \((I–V)\) characteristics obtained from the model and from simulation matched very well (Fig. 16). The model parameters were \(V_p = 96 \, V\) and \(G_0 = 5.67 \times 10^{-5} \, \text{A/V}\).
as computed from the dimensions and doping density of the drift region of the simulated device.

In conclusion, we have presented a simulation study of the CoolMOS™ transistor in both off state and on state. The superior performance of the superjunction structure as compared to the conventional lightly doped drift region in a power MOSFET was explained in terms of electric field profiles. The improved relationship between $R_{on}$ and $V_{g}$ offered by the CoolMOS™ device was discussed. On-state simulations of CoolMOS™ revealed the physical mechanisms responsible for quasi saturation. It was shown that, if the doping density of the drift region is increased, the quasi-saturation effect is prevented from occurring at low gate voltages. Finally, the “pillar” part of the drift region was modeled as a JFET, and good agreement was found between the analytical model and simulation results. In a separate paper [10], we will present an analytic model for the CoolMOS™ transistor, based partly on the simulation results presented here.

**Fig. 16.** $I-V$ characteristics of the pillar part of the drift region for $V_{G} = -25$, $-15$, $-5$, and $0$ V.

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**REFERENCES**


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