Sub-threshold Swing Degradation due to Localized Charge Storage in SONOS Memories

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Abstract — This paper discusses the effect of localized charge storage on sub-threshold swing and threshold voltage in Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) non-volatile memory cells. By analyzing the change in potential contours, it has been shown that the change in sub-threshold swing is correlated to fringing of electric field lines, and hence to the gate-to-substrate capacitance.

I. INTRODUCTION

Subthreshold Swing (SS) degradation is observed when the stored charge is localized in SONOS non-volatile semiconductor memory devices [1]. Understanding the physics of subthreshold swing degradation is important for SONOS memories, used for embedded applications. Degraded sub-threshold swing results in an additional bit line leakage current (on word access) in these memory arrays thus increasing the power dissipation in electronic circuits, loading the peripheral circuitry on chip.

II. SIMULATION RESULTS AND DISCUSSION

Simulations are done on 130nm device of SONOS NVM cells in ISE-TCAD. To understand the effect of localized charge, length of charge packet over the channel ($L_{ch}$) is varied keeping the charge concentration constant (that is, total amount of charge will increase as $L_{ch}$ increases). For the second case, the total charge is kept constant, and $L_{ch}$ is varied. Sub-threshold swing (SS) and $V_t$ are extracted for all the different conditions. Fig.1 shows the schematic of the location of charge packet for a SONOS cell.

![Diagram](image)

Fig.1. Device Schematic used for simulations. $L_{ch}$ is defined as the length of charge packet in the overlap region, which is kept constant through out this work. $L_{ch}$ is defined as the length of charge packet over the channel region, which is varied.

A. $V_t$, SS variation with $L_{ch}$ and charge concentration

It is seen from Fig. 2 that $V_t$ rises rapidly for low $L_{ch}$ values, and then saturates, though the total charge is higher for higher $L_{ch}$. SS degradation depends on charge concentration and $L_{ch}$ (Fig. 3). SS shows maximum degradation for relatively smaller values of $L_{ch}$. The peak value of SS degradation shifts to lower $L_{ch}$ as the charge concentration increases. Variation of SS degradation with constant amount of total charge is shown in the inset of Fig. 3. It is observed that, for the case when the charge is localized, the degradation becomes higher, even when the total injected charge is kept constant. This occurs, as we shall show, due to the fringing of electric field lines for smaller $L_{ch}$ values.

Nomenclature

List of symbols

$q$  Depletion charge (C)  
$C_d$  Depletion layer charge (F/μm)  
$C_{gb}$  Gate to Bulk capacitance (per unit width) (F/μm)  
SS  Subthreshold Swing (mV/decade)  
$L_{ov}$  Length of charge packet in the overlap region, which is kept constant through out this work, (nm)  
$L_{ch}$  Length of charge packet over the channel region, which is varied (nm)  
$\rho_n$  Charge concentration (1/cm$^3$)  
$V_g$  Gate Voltage (V)  
$V_t$  Threshold Voltage (V)  
$\%\delta V_t$  Percentage change in threshold voltage with reference to erased cell $V_t$  
$\%\delta SS$  Percentage change in Subthreshold Swing with reference to erased cell Subthreshold Swing  
$\phi_s$  Surface Potential (V)
Radiation studies reported in 1980's have also studied this phenomenon of lateral non uniform oxide charges (LNU's) causing MOSFET sub-threshold swing degradation [2]-[3], similar to the recently reported results for SONOS non-volatile memories [1]. Degradation due to LNU's was separated from that due to interface traps by methods such as the frequency independent CV stretch out or by low temperature testing, as explained in references [3]-[4].

B. $C_{gb}$ Variation with $L_{ox}$ and charge concentration

In Fig. 4 $C_{gb}$ is plotted as a function of $L_{ox}$ for different charge concentrations. It can be seen that $C_{gb}$ variation with $L_{ox}$ follows an inverse trend as compared to the SS variation. Since a lower $C_{gb}$ would mean reduced gate control, and hence an increased $SS$, in Fig. 5 is plotted percentage change in SS as a function of $1/C_{gb}$. The change in SS is obtained by a change in the charge packet length.

As expected, the change in $C_{gb}$ shows an excellent correlation with the SS variation. As the charge packet length is increased, electric field lines originating on the gate terminate normally on the channel region, with reduced fringing. This argument is supported from the potential plots in the channel region, shown in Fig. 6. The length of the charge distribution from the source end is also shown in this plot for different values of $L_{ox}$. It can be seen that, for smaller values of $L_{ox}$, the potential changes throughout the channel due to fringing, while for the higher $L_{ox}$ case, the change in potential is localized underneath the charge packet.
III. Conclusion

We have studied the effect of charge packet length on the SS degradation in SONOS non-volatile memories. Our 2-D simulation results clearly show that a factor of two or higher sub-threshold swing degradation is expected for charge packet lengths in the range of 10-20 nm for 130 nm gate length SONOS cells. The sub-threshold swing degradation is correlated with the gate fringing fields arising from the charge stored in the nitride. For the first time, we have quantified this fringing in terms of the gate-to-substrate capacitance.

REFERENCES