Channel Engineering for High Speed Sub-1.0 V Power Supply

Deep Sub-micron CMOS

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Abstract
The effects of channel engineering on the device performance have been extensively investigated. The Lateral Asymmetric Channel (LAC) MOSFETs show significantly higher $I_{dsat}$ and $g_m$ at low $V_{gs}$ and superior short-channel performance compared with Double-Halo (DH) and conventional MOSFETs by effectively utilizing the velocity overshoot effects. It is demonstrated that the device switching speed of the LAC device at $V_{DD}=0.6$V is equivalent to that of a conventional device operated at $V_{DD}=1.5$V.

Introduction
Scaling $V_{DD}$ down to sub-1.0 V is the most effective way to reduce the dynamic power consumption. To maintain high current drive and gate switching speed at low $V_{DD}$, low $V_T$ is vital to maximize the gate drive. On the other hand low $I_{off}$ is necessary for small static power [1]. As device dimensions are scaled down to the 0.1 pm regime, velocity overshoot becomes extremely important. Device design that exploits non-equilibrium transport phenomena is an effective way to enhance the device performance [2]-[4]. In this work, a Lateral Asymmetric Channel (LAC) structure is employed to accelerate the tangential electric field at the source side and consequently achieve very high carrier velocity. LAC profile also results in excellent DIBL and $S$, yielding a low $I_{off}$.

Device Fabrication
Both LAC and conventional SOI MOSFETs were fabricated on the same wafer to eliminate potential variations arising from processing differences. Bulk CMOS devices were also fabricated in parallel. The thicknesses of the gate oxide, SOI film, and buried oxide are respectively 3.8nm, 50nm, and 180nm, respectively. Electron beam lithography was used to define the poly fine lines down to 0.06pm. A large angle tilt implant (LATI) was employed to adjust the $V_T$ for both LAC and DH MOSFETs after the poly gate formation while the $V_T$ adjustment of the conventional device was done before the gate oxidation as shown in Fig. 1. The channel implant conditions are given in Table 1. All the dopants were activated by a single RTA anneal at 1020°C for 15s. Low thermal budget Ge pre-amorphization Ti silicidation process was employed with a final $g_{max}$ of 5 $cm^2/V$sec.

Results and Discussion
The carrier transport properties were simulated with an energy balance model for the three channel profiles in Fig. 2. A much higher electron velocity at the source side in LAC device has been achieved compared with the DH and conventional devices (Fig. 3). This high electron velocity is induced by the tangential electric field and its gradient at the source side in the LAC device. The $V_T$ roll-off of the LAC MOSFETs (conventional devices) are less than 60mV (197mV) and 180mV (325mV) down to $L_{off}=0.08$ pm (Fig. 5). The $V_T$ roll-off and DIBL are well controlled by the high doping concentration on the source side in the LAC device, which acts as a dopant barrier limiting the penetration of E-field from drain-to-source. The asymmetric nature of the LAC device is clearly seen in Fig. 6 from the experimental $V_T$ distributions derived from charge-pumping measurements [5]. Much smaller DIBL and $S$ of 94mV and 90mV/decade (158 mV/decade for conventional device) are also obtained in a 0.11um LAC device on bulk substrate (Fig. 7). The LAC device therefore has a lower $I_{off}$. With thinner gate oxide, both DIBL and $S$ will further improve. The high DIBL seen in the reverse mode operation of the LAC device requires some special considerations in circuit design.

Device Performance
Using a Figure of Merit (FOM) of $I_{dsat}/(C_{gs}V_{DD})$, the device performances of the LAC and conventional devices are compared experimentally for both bulk and SOI MOSFETs at fixed $V_{gs}$=1.0V and $V_{dd}$=0.6V (Fig. 10). Both LAC bulk and SOI MOSFETs achieve the same performance at $V_{DD}=0.6$V as their conventional counterparts operated at 1.5V. Excellent short-channel performance also allows the LAC device to have a low $V_T$ while maintaining low $I_{off}$. A comparison of the device performance of the three structures with $V_T$ of 0.15V and 0.25V is made using 2-D device simulations at $V_{gs}$=1.0V ($V_{dd}$=0.6V). For the same $V_T=0.25$V, the LAC device has much better performance compared with DH and conventional devices. Scaling $V_T$ from 0.25V to 0.15V further increases the LAC device performance. In the case of interconnect delay, a FOM of $I_{dsat}/V_{DD}$ gives similar conclusions.

Conclusion
The LAC profile significantly improves device $I_{dsat}$ and gate switching speed by effectively utilizing velocity overshoot effects in deep sub-micron MOSFETs. LAC-MOSFETs have also been shown to exhibit superior short-channel performance and subthreshold characteristics for channel lengths down to the 0.1um regime. These devices are highly suitable for high speed and low voltage/power applications.

Acknowledgments
This work was supported by DARPA.

References

4930813-93-X/99 1999 Symposium on VLSI Technology Digest of Technical Papers
Table 1: NMOS Channel implant conditions

<table>
<thead>
<tr>
<th>Profile</th>
<th>Implant Conditions</th>
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<tbody>
<tr>
<td>CON</td>
<td>B: 12 Kev, 8x10^{13} cm^{-2}</td>
</tr>
<tr>
<td>LAC</td>
<td>BF2: 40 Kev, 4x10^{13} cm^{-2}, tilt=10°</td>
</tr>
<tr>
<td>DH</td>
<td>BF2: 40 Kev, 3x10^{12} cm^{-2}, tilt=10°</td>
</tr>
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Fig. 1. Schematic diagrams of VT-adjustment.

Fig. 2. Channel impurity profiles at 1.5nm away from SiO_x/Si interface. L_{eff}=0.1μm.

Fig. 3. Drift velocity averaged over a depth of 50 nm from Si/SiO_x interface. The inset shows the tangential field (E_t) distributions.

Fig. 4. Subthreshold characteristics for the three devices at V_{DS}=50 mV and 1.5 V with L_{eff}=0.11 μm.

Fig. 5. VT roll-off as a function of effective channel length L_{eff} at V_{DS}=50 mV.

Fig. 6. Experimental VT profiles along the channel as obtained from the Charge Pumping measurements in pre-stress. L_{eff}=0.11μm.

Fig. 7. Measured DIBL as a function of L_{eff}.

Fig. 8. Measured I_{DS} - V_{DS} characteristics for the LAC and conventional MOSFETs. V_{GT}=V_{GS}-V_{T,off}.

Fig. 9. Measured g_m as a function of L_{eff}.

Fig. 10. Figure of Merit (FOM) vs. power supply V_{DD}. V_{GT}=V_{DS}+V_{DD} - (a) BULK; (b) SOI.

Fig. 11. Figure of Merit (FOM) vs. power supply V_{DD} for different structures and VT. V_{GS}=V_{DS}+V_{DD}.