A Simplified Control Strategy for a High Power Low Distortion Synchronous Link Converter Var Compensator

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Abstract—A high power low distortion static var compensator is proposed in [1]. The harmonics are eliminated by incorporating a low power IGBT based controlled current auxiliary converter in conjunction with a high power GTO based converter. The current reference required by the auxiliary converter is calculated by an involved procedure which makes the overall compensation process complicated. In this paper a simplified control scheme for the var compensator of [1] is proposed. Effectiveness of the proposed scheme is investigated for a case where the var compensator is specifically used for load compensation and also for the case where it is used as a general purpose var generator. Detailed simulation studies of the schemes are presented. Experimental results obtained from a laboratory prototype are provided to demonstrate the viability of the proposed method.

Keywords—SLCVC, SVC, Harmonic elimination, Load Compensator, Var Generator.

I. INTRODUCTION

The traditional methods of reactive volt-ampere compensation consisting of switched capacitor or fixed capacitor and phase controlled reactor coupled with passive filters are increasingly being replaced by new approaches utilising the concept of Synchronous Link Converters [2]. This new class of compensators which have earned overwhelming response from the researchers, is known by several terminologies such as ‘Var Generators’ [3], ‘Advanced Static Var Generators’ [4], Synchronous Solid State Var Compensators’ [5], ‘PWM Inverter Var Compensator’ [6], ‘STATCOM’, etc. In this paper it is referred to as Synchronous Link Converter Var Compensator (SLCVC). Although this class of compensators provide improved performance over the traditional methods of var compensation, it still has the serious drawback of injecting low order harmonics into the utility. The problem becomes acute at high power levels. Several PWM techniques of harmonic elimination [5,6,7] cannot be realised at high power levels due to switching frequency limitation of high power devices. To reduce low frequency harmonics either parallely operated converters [8,9,10,11,12] or multilevel converters [13,14,15,16,17] are being used. The disadvantages of parallelly operated converter topology are – 1) the transformer connection at the input side of the compensator becomes complicated and bulky, 2) as the number of harmonics to be eliminated increases, the number of parallel units are also required to be increased which implies poor performance/cost ratio and 3) the structure of control becomes complicated.

The limitations of the multilevel converter topology are – 1) as the number of harmonics to be eliminated increases the performance/cost ratio falls, 2) voltage unbalance among the different levels of capacitors, 3) increase in active component count (diode clamp topology) or increase in passive element count (flying capacitor topology) and 4) complexity in control.

Moreover in the above cases, the harmonics are eliminated in offline mode of control as a result of which, a relatively small error in the hardware realisation of device switching instants results in a significant increase in the harmonic content.

In order to overcome the above mentioned limitations, a novel technique of harmonic elimination is proposed in [1] wherein low frequency high power devices and high frequency low power devices are combined to extract a superior performance. The basic philosophy of the scheme is that two converters sharing a common dc bus are used in parallel, of which one is realised by GTOs while the other one is realised by high frequency devices like IGBTs, MOSFET or BJTs depending on the current level to be handled. The GTO converter (or the main converter) is operated with PWM control based on selective harmonic elimination technique so that only few low order harmonics get eliminated. Since the number of harmonics to be eliminated by this main converter is less, the switching frequency also remains low. The high frequency parallel or auxiliary converter is operated in the current controlled mode to eliminate the next higher order harmonics generated by the main compensator. The control methodology ensures that the fundamental reactive current demand is supplied only by the GTO based converter. The auxiliary converter compensates for the harmonics generated by the main converter. Since the auxiliary converter does not handle the fundamental reactive current, its KVA rating remains low. In [1], this scheme of harmonic elimination is validated through simulation studies. In this paper the experimental results of the scheme proposed in [1] are provided after presenting the underlying concept of the scheme. The control scheme proposed in [1], requires an involved procedure to determine the reference current for the auxiliary converter. In the scheme presented here, this reference current is determined by having a second closed loop around the converters. This results in reduction in hardware requirement and cost, and leads to an overall improvement in system reliability due to simplicity in hardware realisation. Effectiveness of the proposed scheme is
investigated for a case where it is specifically utilised for load compensation. The advantage of this mode of operation is that the load harmonics also get eliminated. The scheme is also studied for the case where it is used as a general purpose var generator which can be utilised either for load compensation or for bus voltage support. The viability of the scheme is confirmed through detailed simulation and experimental studies.

The idea of utilising a low power auxiliary converter in conjunction with a high power converter for harmonic elimination was first proposed in connection with Synchronous Link Voltage Source Converters [18,19]. The idea of incorporating auxiliary compensator has also been reported in [20]. The main limitation of the approach followed in [20] is that the control structure is quite involved. Also the presence of two reactive volt-ampere calculators and two filters in the control structure has a detrimental effect on the response of the system. Moreover, there is a substantial increment in the passive and active component count. In [21], the two converters having separate dc buses are controlled independently, as a result the control structure becomes complicated. The scheme presented here is free from the above limitations.

II. OPERATING PRINCIPLE

The power circuit configuration of the scheme is shown in Figure 1. The main converter is operated with selective harmonic elimination technique, so as to eliminate 5th, 7th, and 11th harmonics. Hence the switching frequency of the main compensator devices is 450 Hz. The switching instants are fixed and the fundamental component of the compensator current is controlled by controlling the magnitude of dc link voltage rather than controlling the modulation index. The auxiliary converter is operated in current controlled mode and provides online elimination of the higher order harmonics generated by the main compensator. Three reference sinusoids, $i_{ref(1)}$, $i_{ref(2)}$, and $i_{ref(3)}$, having equal amplitude, $I_f$, and in phase with the line to neutral voltages, $v_{m1}$, $v_{m2}$, and $v_{m3}$ are synthesised. The source currents $i_{s1}$, $i_{s2}$, and $i_{s3}$ are forced to follow these references within a hysteresis band. The source currents are sensed and compared with the respective reference sinusoids. The error thus obtained decides the switching pattern of the auxiliary converter devices. Suppose at some instant of time $i_{s1}$ is less than $i_{ref(1)}$. In order to increase $i_{s1}$, the lower device of phase-A of the auxiliary converter, $S_1$ is turned on so that the auxiliary compensator current, $i_{aux}(a)$ increases. Now from Figure 1,

$$i_{s1} = i_{ref(1)} + i_{aux}(a) + i_{aux}(a)$$

therefore, $i_{s1}$ increases with $i_{aux}(a)$. When $i_{s1}$ hits the upper bound of the hysteresis band, $S_1$ is turned off and the lower device of phase-A of the auxiliary converter, $S_2$ is turned on so that the auxiliary compensator current, $i_{aux}(a)$, decreases. The same technique is followed for controlling the current of the other phases. Thus by controlling the switching pattern of the auxiliary converter, the source current is rendered near sinusoidal. As the source currents are forced to follow sinusoidal references, the load harmonics if present also get eliminated. Oscillogram records of the various steady state waveforms obtained are shown in Figures 2 to 6. Figure 2 depicts the behaviour of the compensator when the auxiliary compensator is disconnected while Figures 3 and 4 show the behaviour with the auxiliary compensator. Figure 5 shows the harmonic spectrum of the ph-A source current with the auxiliary compensator while Figure 6 shows the spectrum without the auxiliary compensator.

III. CONTROL STRUCTURE

The schematic control block diagram of the compensator is shown in Figure 7. Since var supplied by the compensator is proportional to the magnitude of the dc link volt-

Fig. 5. Aux. Comp. Connected: Harmonic Spectrum of the Ph-A Source Current. (Freq. Scale: 250Hz/div)

Fig. 6. Aux. Comp. Disconnected: Harmonic Spectrum of the Ph-A Source Current. (Freq. Scale: 250Hz/div)

Fig. 7. Control Block Diagram of the SLCVC as a Load Compensator.

actual practice such a precise choice of the controller parameters is not possible. As a result, some part of the real power required to maintain the dc link voltage will flow through the auxiliary compensator. Since the real power involved is insignificant and the auxiliary compensator handles only a fraction of this power, the increment in the VA rating of the auxiliary compensator is negligible.

IV. SIMULATION STUDIES

Detailed simulation studies are carried out to predict the performance of the proposed compensator. A dedicated computer program is developed for the purpose and simulation results are presented. The value of the dc link capacitance is 400μF and the hysteresis window height is kept 1.0 Amp. The values of the two inductors are $L_m = 20$ mH; $L_a = 12$ mH. Figure 8 shows the transient behaviour of the three phase compensator for a step change in reference dc link voltage from 1200V to 1900V and a simultaneous change in load from $(1.67 + j6.93)KVA$/phase to $(1.67 + j17.0)KVA$/phase.

From the simulated results it can be inferred that superior compensation performance can be obtained by virtue of the proposed compensation technique. The steady state volt-ampere rating of the auxiliary converter is found to be around 5% of the main converter. Moreover, it is found that the transient response of the scheme is superior. This is due to the fact that during the transient period the auxiliary compensator supplies the necessary var demand of the load. This results in the increment of the auxiliary converter current during transient period and hence of its transient volt-ampere rating. This increment in transient volt-ampere rating of the auxiliary converter can be explained as follows: If there is an increment or decrement in var demand, the var calculator increases or decreases the dc link voltage reference. The actual dc link voltage responds to this change with a finite response delay. But the controller is forcing the auxiliary converter to control its own currents so that the source currents remain in phase
with the respective source voltages. Thus during the transient period the deficit amount of var which the main compensator is not able to supply, is being supplied by the auxiliary compensator. As the peak current rating of a device is almost twice that of its continuous current rating, drawing of high current for a short duration from the auxiliary converter is permissible. However, this can be detrimental for the high frequency devices in certain high power applications involving fast and large change in var demand. This problem is addressed by operating the proposed scheme as a var source which is presented in Section V.

V. PROPOSED SLCVC AS VAR GENERATOR

The control strategy discussed in the previous section maintains a sinusoidal current source by controlling the auxiliary converter switchings. As a result, the load nonlinearities if present also get compensated by the auxiliary compensator. Therefore, when the source is supplying a nonlinear load, auxiliary compensator has to compensate load harmonics in addition to the harmonics generated by the main compensator. Since in high power applications the percentage of load harmonics is generally insignificant compared to the load reactive current, percentage increase in the volt-ampere rating of the auxiliary converter will not be considerable. However, if the load nonlinearities are significant, the volt-ampere handled by the auxiliary compensator may increase beyond the rating of high frequency devices. In that case, instead of controlling the source current, the overall compensator current is sensed and controlled so that the auxiliary compensator compensates only the harmonics generated by the main compensator. Further this approach of control ensures that there is no significant increase in the transient volt-ampere rating of the auxiliary converter. This control technique is discussed in detail in this section. Here the proposed SLCVC is looked upon as a general purpose var generator which can be used either for load compensation or for bus voltage support applications.

A. Operating Principle

The power circuit configuration of the var generator is shown in Figure 9. The principle of operation remains almost the same as explained in Section II. The currents drawn by the compensator unit, \( i_{(a)} \), \( i_{(b)} \) and \( i_{(c)} \) are sensed and made to follow three reference currents, \( i_{(a)} \), \( i_{(b)} \) and \( i_{(c)} \) by controlling the switchings of the auxiliary compensator devices. The control block diagram of the scheme acting as a var generator is shown in Figure 10. The PI Controller-2 supplies the information regarding the amplitude of the real component of the overall compensator.
sator current, $I_{cp\text{ (real)}}$ required to maintain the necessary dc link voltage. As the reactive current handled by the compensator is proportional to the magnitude of the dc link voltage, the amplitude of the quadrature component of the compensator current, $I_{cp\text{ (quad)}}$ is obtained by multiplying $V_{dc}$ with a proportionality factor, $K$. The dc link voltage is compared with a threshold voltage, $V_{th}$ to get the data regarding the phase relationship (+90° or -90°) between the quadrature component of the compensator currents and the utility voltages. When $V_{dc} < V_{th}$, the sign of $I_{cp\text{ (quad)}}$ is reversed so that the reference current lags the utility voltages by 90°. For $V_{dc} > V_{th}$, the sign of $I_{cp\text{ (quad)}}$ is left unchanged which ensures that the reference currents lead the utility voltages by 90°. The proportionality factor, $K$ and $V_{th}$ depend on the system parameters, $V_s$ and $L_m$. The reference currents are then given by:

$$i_{ref(a)} = I_{cp\text{ (real)}} \cos(\omega t) + I_{cp\text{ (quad)}} \cos(\omega t + 90°)$$  \hspace{1cm} (2)

$$i_{ref(b)} = I_{cp\text{ (real)}} \cos(\omega t - 120°) + I_{cp\text{ (quad)}} \cos(\omega t + 90° - 120°)$$  \hspace{1cm} (3)

$$i_{ref(c)} = I_{cp\text{ (real)}} \cos(\omega t + 120°) + I_{cp\text{ (quad)}} \cos(\omega t + 90° + 120°).$$  \hspace{1cm} (4)

When the compensator is utilised for bus voltage control, the r.m.s bus voltage is sensed and compared with the reference bus voltage, and the error is utilised to set $V_{dc\text{ (ref)}}$. While this scheme is to be used for load compensation, the reactive volt-ampere calculator sets $V_{dc\text{ (ref)}}$. Simulation studies are carried out with $L_{m(a,b,c)} = 20\text{mH}$, $L_{m(a,b,c)} = 12\text{mH}$ and dc link capacitor, $C = 400\mu\text{F}$. The transient response of the scheme for a step change in $V_{dc\text{ (ref)}}$ from 1200V to 1900V is shown in Figure 11.

VI. EXPERIMENTAL VERIFICATION

The proposed control strategy is experimentally verified by operating the SLCVC as a load compensator. During testing, the load current of each phase is maintained at (0.5 ± 0.0)Amp and the reference dc link voltage is changed from 150V to 180V. Figures 12 and 13 depict the compensator performance for this condition. It can be seen from Figure 12 that when the dc link voltage is 150V, the auxiliary compensator is drawing a leading current from the source. This is because the reference dc link voltage is inadequate for the main compensator to supply the full var demand of the load. But 180V is almost adequate for the main compensator to fully compensate the load. Hence the auxiliary compensator draws reduced current at this voltage. Figures 14 and 15 show compensator performance when a step change of 180V to 150V is introduced in the reference dc link voltage.

VII. CONCLUSIONS

A simplified control scheme of a high power low distortion SLCVC is proposed. Superior performance characteristics are obtained by effectively combining high power low frequency and low power high frequency switching devices. Detailed simulation studies are carried out to demonstrate the effectiveness of the scheme. Viableity of the scheme
is confirmed through experimental results obtained from a scaled down laboratory prototype.

REFERENCES