A NOVEL QRDCL CIRCUIT FOR ZERO VOLTAGE SWITCHED INVERTER

*MD Bagewadi, *BG Fernandes and **RVS Subrahmanyam
*Department of Electrical Engineering, Indian Institute of Technology, Bombay
Powai, Mumbai - 400 076, India.
**NCE, INS Shivaji, Lonavla-410402, India.

ABSTRACT

This paper presents an alternate quasi-resonant dc link (QRDCL) circuit for soft switched inverters which does not require paralleling of a charged capacitor with another charged capacitor or a voltage source. The circuit momentarily pulls down the DC link voltage to zero as commanded by the control circuit to facilitate zero voltage switching (ZVS) of inverter devices. Operation of this circuit is independent of load current. The circuit is snubberless and offers true PWM capability. The paper covers description of the circuit, operating principles, detailed analysis of various modes and design considerations. Feasibility and operating principles of the circuit have been verified by simulation using PSPICE.

1. INTRODUCTION

In the last decade a number of quasi-resonant zero voltage switching (ZVS) DC link inverters have been reported [1 - 5]. The quasi-resonant circuit pulls the DC link voltage momentarily to zero as commanded by the control circuit to facilitate zero voltage switching of the inverter devices. [1 - 4] use a series switch in the DC link which carries full load current. Voltages stresses are strictly 1.0pu in these circuits. An alternative is to use an inductor in the DC link with a clamp [5] in which zero voltage notches necessitate the DC link voltage to be higher than the source voltage for volt second balance in the inductor. At 25 kHz switching frequency, the DC link voltage is marginally higher (1.06 pu) than the source voltage. This paper presents an alternate ZVS quasi-resonant DC link inverter which does not involve paralleling of a charged capacitor with another charged capacitor as in [5] or a voltage source as in [1 - 4]. The load current does not charge or discharge the resonant capacitor and hence it’s operation is independent of load current.

2. PROPOSED CIRCUIT

The proposed circuit is shown in fig 1. Capacitor \( C_1 \) is much larger than \( C_2 \) and its voltage may be assumed constant at the nominal steady state value \( V_{DCN} \). During normal operation \( Q_1 \) is on and \( C_2 \) is fully discharged. Capacitor \( C_1 \) is the main DC link capacitor which provides constant voltage for the inverter. Switch \( Q_1 \) is turned off at zero voltage, followed by turn on of \( Q_2 \) with current to initiate resonance between \( C_2, C_1, L_2 \). Capacitor \( C_2 \) is charged to \( -V_{DCN} \) in a quarter cycle of resonance. DC link voltage at this instant becomes

\[
V_{DC}(t) = V_{C1}(t) + V_{C2}(t) = 0
\]

\( V_{DC} \) is clamped to zero by the inverse parallel diodes of the inverter devices. \( Q_2 \) is turned off with zero voltage at this instant. The inductor current \( I_{L2} \) decays to zero through \( C_2, D_3, L_1 \) and \( L_2 \). Duration of zero voltage of the DC link lasts as long as \( C_2 \) remains charged to \( -V_{DCN} \). Inverter devices can be switched on or off during this zero voltage duration. After some delay, long enough to turn on or off inverter devices, \( Q_3 \) is turned on with zero current and zero voltage initiating resonance between \( C_2 \) and \( L_2 \). When \( V_{C2} \) reaches zero \( Q_3 \) is turned off at zero voltage. At this instant the dc link voltage is restored to \( V_{DCN} \). Inductor current \( I_{L2} \), which has attained negative maximum value decays to zero through \( L_2, D_3, C_1 \) and \( D_1 \). Thus the energy stored in \( L_2 \) is returned to \( C_1 \). Switch \( Q_1 \) can now be turned on at zero voltage. The equivalent circuit for the duration of switching is shown in fig 2. The load inductance is much larger than \( L_4 \) and \( L_1 \) is much larger than \( L_2 \) and hence the inverter can be replaced by a current source \( I_0 \) as shown in fig 2.

3. MODES OF OPERATION

The circuit can be analysed using the equivalent circuit shown in fig. 2. The current \( \Delta I = I_{L4} - I_0 \) which can be assumed constant for the duration of soft switching, excites the quasi-resonant circuit. Relevant waveforms are shown in fig 5.
MODE 0 (Prior to 
\( t_0 \)): The circuit is in steady state 
with \( Q_1 \), \( Q_2 \) and \( Q_3 \) off and \( C_2 \) fully discharged.

MODE 1 (\( t_0 \) to \( t_1 \)): Switch \( Q_1 \) is turned off at zero voltage 
at \( t_0 \) and \( Q_2 \) can now be turned on.

MODE 2 ((\( t_1 \) to \( t_2 \))): Switch \( Q_2 \) is turned on at zero current 
at \( t_1 \) to initiate resonance between \( C_1, C_2 \) and \( L_2 \). The 
equivalent circuit for the mode is shown in fig 3. This mode 
starts with initial condition \( V_{C1} = V_{DCN}, V_{C2} = 0 \) 
and \( I_{L2} = 0 \). The expressions for \( V_{C2}, I_{L2}, V_{C1} \) 
and \( V_{DC} \) for this mode can be written as

\[
V_{C2}(t) = \left( \frac{C_{eq}}{C_2} \right) V_{DCN} \cos \omega t + [\Delta I/(C_2\omega)] \sin \omega t
\]

\[
I_{L2}(t) = \sqrt{\left( \frac{C_{eq}}{L_2} \right)} V_{DCN} \sin \omega t + \Delta I / (1 - \cos \omega t)
\]

\[
V_{C1}(t) = \left( \frac{C_{eq}}{C_1} \right) V_{DCN} \cos \omega t + \Delta I / (1 - \cos \omega t) + V_{DCN}
\]

\[
V_{DC}(t) = V_{DCN} \sin \omega t + \Delta I / (C_{eq}) \sin \omega t + \Delta I / C_{eq}
\]

Where, \( C_{eq} = \frac{(C_1)(C_2)}{C_1+C_2} \) and 
\( \omega_0 = \sqrt{\left( 1/(L_2, C_{eq}) \right)} \)

\( V_{DC}(t) \) becomes zero when, 
\( \cos \omega t = \Delta I / (1 - \cos \omega t) \). It can be seen from (4) 
that for small \( \Delta I, V_{DCN} \) becomes zero for \( \omega t = \pi/2 \). 
This mode ends when \( V_{DC} \) becomes zero at \( t_2 \). Switch \( Q_2 \) is 
turned off at zero voltage at \( t_2 \). \( V_{C2} \) and \( I_{L2} \) at the end of 
this mode can be written as

\[
V_{C2} = -V_{DCN}
\]

\[
I_{L2} = \sqrt{\left( \frac{C_{eq}}{L_2} \right)} V_{DCN}
\]

MODE 3 (\( t_2 \) to \( t_3 \)): Current \( I_{L2} \) decays to zero through \( L_2, D_2, C_1 \) 
and \( D_1 \) almost linearly as \( C_1 \) is very large. 
Energy stored in \( L_2 \) is completely transferred to \( C_1 \). This 
mode ends when \( I_{L2} \) reduces to zero at \( t_3 \). At \( t_3 \), \( Q_3 \) 
is turned on at zero voltage and the quasi-resonant cycle 
comes to an end.

4. SIMULATION RESULTS

The circuit shown in fig 2 has been simulated in PSPICE. 
\( V_i = 500V, L_2 = 10\mu H, C_1 = 100\mu F, C_2 = 10nF \), 
\( L_1 = 10mH \) and switching frequency chosen is 40kHz. The simulation 
results, shown in fig. 6 are found to be in agreement with 
the analytical results for all possible loading conditions.

5. DESIGN CONSIDERATIONS

The duration of zero voltage of the DC link is controlled 
by delaying the turn on of \( Q_3 \) at the end of mode 4 at \( t_5 \). 
\( L_2 \) and \( C_2 \) are so selected as to achieve quick transition of 
the DC link voltage from \( V_{DCN} \) to zero and from zero 
back to \( V_{DCN} \) in the quasi-resonant cycle.

Let \( 2(t_5-t_4) = 2(t_4-t_3) = \pi \sqrt{(C_2/L_2)} = 1\mu s \) 
(8)

The energy storage and transfer involved in the quasi-resonant stage is \( W_{eq} = 0.5 \left( C_2 V_{DCN}^2 \right) \)
In order to limit this \( C_3 \) is chosen small, say \( 10nF \). 
Knowing \( C_3, L_2 \) can be found from (8). Also, maximum 
energy stored in \( L_2 \) is 
\( 0.5(L_2 I_{max}^2) = 0.5 (C_2 V_{DCN}^2) \)
and hence the maximum current in the quasi resonant 
stage is

\[
I_{max} = \sqrt{(C_2/L_2)} V_{DCN}
\]

All the devices in the quasi-resonant circuit namely \( Q_3, Q_2, D_2, D_3, C_2 \) and \( L_2 \) 
experience a maximum voltage stress of \( V_{DCN} \) and 
maximum current of

\[
I_{max} = \sqrt{(C_2/L_2)} V_{DCN}
\]
6. CONCLUSION

A novel quasi-resonant circuit for zero voltage switched inverters has been designed and simulated using PSPICE. The circuit offers an alternate approach to zero voltage switching quasi-resonant DC link circuits in which paralleling of a charged capacitor with another capacitor or a voltage source is avoided. In addition the circuit offers all advantages of many other ZVS QRDCL inverters like snubberless operation and true PWM capability. Operating principles for all loading conditions have been verified by simulation.

REFERENCES
