High field characteristics of metaloxidesemiconductor capacitors with the silicon in inversion

R. M. Patrikar, R. Lal, and J. Vasi

Citation: J. Appl. Phys. 73, 3857 (1993); doi: 10.1063/1.352896

View online: http://dx.doi.org/10.1063/1.352896

View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v73/i8

Published by the American Institute of Physics.

Related Articles

Iron-phthalocyanine molecular junction with high spin filter efficiency and negative differential resistance

Length dependence of the resistance in graphite: Influence of ballistic transport

Theory of quantum energy transfer in spin chains: Superexchange and ballistic motion

Drift velocity peak and negative differential mobility in high field transport in graphene nanoribbons explained by numerical simulations

Field dependent electrical conduction in HfO2/SiO2 gate stack for before and after constant voltage stressing
J. Appl. Phys. 110, 084104 (2011)

Additional information on J. Appl. Phys.

Journal Homepage: http://jap.aip.org/

Journal Information: http://jap.aip.org/about/about_the_journal

Top downloads: http://jap.aip.org/features/most_downloaded

Information for Authors: http://jap.aip.org/authors
High field characteristics of metal-oxide-semiconductor capacitors with the silicon in inversion

R. M. Patrikar, R. Lal, and J. Vasi
Department of Electrical Engineering, Indian Institute of Technology, Bombay, Bombay 400076, India
(Received 6 July 1992; accepted for publication 17 December 1992)

Degradation of the gate oxide is often studied by stressing of metal-oxide-semiconductor (MOS) capacitors. Usually the MOS capacitor is stressed in accumulation to avoid the complications due to a voltage drop across the depletion layer if stressed in inversion. High field stressing studies for MOS capacitors with the silicon in inversion are presented in this article. Our observations show that in this mode, silicon properties (mainly minority carrier generation lifetime) play an important role.

I. INTRODUCTION

Dielectric quality of gate oxides is an important consideration in metal-oxide-semiconductor (MOS) devices. It is now well known that degradation of the gate oxide with high-field stressing or hot carrier injection is a wearout process which depends, along with other things, on the number of carriers injected in the oxide. \(^1\) The wearout properties of silicon depend upon the polarity of the stressing in dc and pulsed stressing. Although the MOS structure in a metal-oxide semiconductor field effect transistor (MOSFET) has the silicon in inversion, high-field degradation has normally been studied in MOS capacitors by stressing the device with the silicon in accumulation. This is because the flux of carriers, which are primarily electrons through the structure, is then limited by tunneling at the cathode. The characteristics for Fowler–Nordheim (FN) tunneling are well known, \(^6\) hence the task of correlating wearout with current through the structure is simplified. Only a few studies of degradation with the silicon in inversion have been reported because the current-voltage characteristics (I-VC) of MOS capacitors with the silicon in inversion are not well understood. In this article we examine high-field characteristics of MOS capacitors with the silicon in inversion.

Breakdown in a MOS capacitor is a complex process that depends not only on the properties of the bulk dielectric which determine wearout, but also on the contacts which determine charge injection into the dielectric. For any particular dielectric, it is the properties of the electrodes (like work function, roughness, areal homogeneity of various parameters like oxide charge, interface states, etc.) that determine the variability in I-VCs and thence breakdown characteristics.

The contact between an electrode and an insulator is normally blocked because of the large conduction and valence band discontinuities at the interface. However, for large voltages applied across the structure, carriers could get tunnel injected into the dielectric. Normally, for the MOS structure, electrons get injected from the cathode because of the smaller barrier and effective mass compared to those for holes. The limiting factors that determine the I-VC of the structure could be: (i) supply of carriers from the electrodes, (ii) tunneling to the corresponding band in the dielectric, and (iii) drift in the dielectric if only one electrode injects carriers or drift recombination if both electrodes inject carriers.

For the MOS capacitor at room temperature drift of electrons (which predominantly carry the current in the oxide) is not a limiting factor. When the metal (or heavily doped polysilicon) gate is the cathode, supply of electrons is also not a limitation and the I-VC obeys the FN relation. When the semiconductor is the cathode, the supply of electrons depends on whether the semiconductor is in accumulation (N type) or in inversion (P type). In the former case, the supply of electrons is not a limitation and the FN relation is obeyed; while for the latter case, supply of electrons could be a limitation and could control the I-VC. Carrier generation and avalanche multiplication in the semiconductor need to be considered. Besides, trapping of carriers in the dielectric needs to be considered to explain changes in the I-VC with stress time.

II. EXPERIMENT

The samples used in this study were metal gate MOS capacitors with an oxide thickness of 400 Å. The substrate was 1 Ω cm (100) P-type Si. The gate oxide was grown in O\(_2\) at 950 °C followed by a 20 min anneal in nitrogen at the same temperature. Aluminum evaporation was done in an electron beam evaporation system. Square dots of 1 mm\(^2\) were formed by photolithography. The back oxide was etched and aluminum was evaporated for the back contact. Post-metallization anneal was performed at 450 °C for 30 min in nitrogen.

The capacitors were stressed by three techniques: staircase voltage, constant voltage, and constant current. For the constant voltage and constant current stresses; the current through and the voltage across the structure are, respectively, observed as a function of time. For the staircase voltage stress, current measurement has been made after the displacement current decays. Since these are the techniques widely used for high field stressing, understanding the transients and characteristics for these cases would help give a better model of wearout with stress time. The configuration used to stress the device consisted of a Keithley 220 current source for constant current stressing with a Keithley 619 electrometer to monitor the voltage,
and a Keithley 617 electrometer/voltage source for staircase voltage-ampere stressing as well as for constant voltage stressing. The data acquisition and plotting was done with a HP 9826 computer.

III. RESULTS AND DISCUSSION

A. Staircase voltage stress

Figure 1 shows the I-VC taken in inversion with a voltage staircase. There are two different regions. Initially, the current is small and controlled by tunneling but after some voltage it is limited by supply of the carriers from silicon. Initially, the depletion width is small since the generation and diffusion currents supply the minority carriers that tunnel through. The current through the structure is then limited by FN tunneling and obeys the relation,

$$J = AE_0^2 \exp \left(-\frac{B}{E_0}\right),$$

where A & B are constants for FN tunneling at the semiconductor oxide interface and $E_0$ is the field at the oxide-semiconductor interface. Assuming an almost uniform field across the oxide, $E_{ox} - V_{ox}/t_{ox}$, where $V_{ox}$ is the voltage across the oxide and $t_{ox}$ is the thickness of the oxide.

For larger voltages the semiconductor has to go into deep depletion to generate the necessary number of carriers that tunnel through. In this case, the generation current is given by

$$J = \int_{w_m}^{w} \frac{q n_i}{\tau_s(x)} dx + q n_i s + \frac{q n_i^2 D_n}{N_d L_n},$$

where $J$ is the current density through the structure, $q$ the electronic charge, $w$ the depletion width when the potential drop across the semiconductor is $V_s$, $w_m$ the depletion width at strong inversion, $n_i$ the intrinsic concentration, and $\tau_s$ the generation lifetime, $s$ is the surface recombination velocity which depends on the interface state density, and $D_n$ and $L_n$ are diffusion coefficient and diffusion length of minority carriers.

At steady state, the generation current is equal to the tunnel current. Therefore,

$$\int_{w_m}^{w} \frac{q n_i}{\tau_s(x)} dx + q n_i s + \frac{q n_i^2 D_n}{N_d L_n} = AE_0^2 \exp \left(-\frac{B}{E_0}\right).$$

Also

$$V_s + V_{ox} = V.$$  (4)

These equations can be solved iteratively if $\tau_s$ is known and the constants A and B are known. The generation lifetime was found independently by the constant capacitance method and the value found to be 278 ns. We see in Fig. 1 that the fit to experiment is reasonable.

B. Constant current stress

The other commonly used stress technique is constant-current stressing which is widely used for wafer level reliability (WLR) studies. In these experiments devices were stressed with a constant current source and the voltage transient across the structure observed. If the devices have a large generation lifetime, then the constant current source will have to apply the voltage across the depletion layer such that Eq. (2) is satisfied. Also it will have to apply a voltage across the oxide such that Eq. (1) is satisfied. However at higher currents it is possible that the semiconductor will be forced into avalanche breakdown to supply the current. This is shown in Fig. 2, where curve (a) is the voltage transient for a low constant current that does not require the semiconductor to go into avalanche breakdown while curve (b) is for a higher current that forces the semiconductor into breakdown. In the latter case the transient is noisy probably due to the fluctuations of depletion widths as microplasmas turn on and off. When the forced current is not large enough to cause avalanche breakdown, the initial voltage across the structure can be obtained by using Eqs. (1), (2), and (4).
The calculated voltages agree at $t=0$ with the experiment (see Fig. 2). The capacitor used for curve (b) had a lifetime of 2 $\mu$s. The calculations [Eq. (3)] also show that with a lifetime of 2 $\mu$s the voltage across the depletion layer will be more than $10^5$ V for 0.1 mA/cm$^2$ current through the structure. However, the silicon (doping of the substrate, $N_a=1.6 \times 10^{16}$/cm$^3$) will go into avalanching at about 40 V. The voltage required across the oxide is 38 V [Eq. (1)]. Thus the voltage across the MOS capacitor required for this current is about 78 V (depending on the breakdown voltage of silicon). The observed voltage is 74 V (Fig. 2), which is close.

However, the increasing transient after the initial part in Fig. 2 can only be explained with trap generation and trapping in the oxide and interface state generation. Both electron and hole trapping does occur for low currents. We observe that the voltage across the structure increases (Fig. 2) to maintain the same current through it, and therefore electron trapping dominantly controls the electric field.

C. Constant voltage stressing

Though used for time dependent dielectric breakdown studies, constant voltage stressing is seldom used for stress experiments since interpretation of results is more involved compared to either the constant current stress or the staircase voltage stress. However, in this case too, the early phase of the current transient with a constant voltage stress applied across the structure can be estimated from a knowledge of the lifetime in the silicon. Again Eq. (3) can be used to predict current. This equation shows that a smaller current will flow through a capacitor with higher generation lifetime (Fig. 3). However, unlike the constant current stress, straightforward calculations cannot be done because the current through the structure and the field in the silicon and oxide are not known. However solutions of Eqs. (3) and (4) can be found iteratively. These calculations predict the current $7.2 \times 10^{-6}$ A/cm$^2$ for a capacitor which has a lifetime of 48 ns and $5.4 \times 10^{-6}$ A/cm$^2$ for the capacitor which has a lifetime of 62 ns.

IV. CONCLUSION

The $I$-$V$ characteristics and voltage and current transients of MOS structures stressed in inversion have been studied. The $I$-$V$ characteristics can be explained by accounting for the drop across the silicon which is dependent on the carrier lifetime in it. The early parts of the voltage and current transients for constant and voltage stresses, respectively, can also be obtained after estimating the drop across the silicon if the latter is not forced into the avalanche region during stressing. Quantitative estimates of the full transients are not possible because these depend on bulk oxide and interface trap generation, models for which are not yet available. However accounting for the drop across the depletion region should help interpret some experiments in the literature for devices that have been stressed in inversion. For example, Rajdocic has mentioned that the voltage required to provide the desired current (1 $\mu$A) was typically 75 V in inversion whereas accumulation stress required approximately 45 V. This can now be understood quantitatively. Similarly when oxide is voltage stressed it is found that degradation is much greater during accumulation. Our results show that during the inversion most of the voltage is across the silicon depletion layer and thus oxide does not suffer high field stress.

ACKNOWLEDGMENTS

The support of the Ministry of Human Resource Development under its Thrust Area Programme in Microelectronics is gratefully acknowledged.