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Degradation of oxides in metal-oxide-semiconductor capacitors under high-field stress

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High-field effects in metal-oxide-semiconductor capacitors have been studied in detail. A comprehensive set of experiments, stressing identically fabricated capacitors on both P-type and N-type silicon, both in accumulation and in inversion, has been made to study defect generation in the oxide at high fields. There is clear experimental evidence that both bulk hole and electron traps are generated under all stress conditions. High-field prebreakdown properties depend mainly upon the dynamics of generation of traps, trapping and detrapping at these and in previously existing traps. It has been found that of several processes, some dominate, depending upon the type of silicon and polarity during stressing, and this is also true for the final breakdown mechanism. In this paper the dominant mechanisms are identified for each of the field stress conditions that have been studied.

I. INTRODUCTION

Previously, oxide strength had been limited by gross defects, which caused early breakdown. However, for defect-free oxides working under increased fields, wear-out mechanisms have become important. A good understanding of the physical effects resulting due to the application of large electric fields applied to thin oxides is needed. Extensive work has been done in this direction.

Despite numerous experiments done to investigate the effects of high fields on the metal-oxide-semiconductor (MOS) system, there is no consensus on the models to explain the characteristics during and after stressing. This is because the effect of high fields depends upon a number of factors. For example, high-field characteristics depend upon the range of fields used during stressing and previous stress history. They also depend upon the quality, type, and orientation of substrate, oxidation, and annealing temperatures, type of contact used, morphology of the metal, sintering temperature, and on incorporation of foreign atoms in the structure. Furthermore, our experiments show that these characteristics also depend upon whether the silicon is in inversion or in accumulation during stressing.

Totally diverse conclusions have been presented in the literature. It seems that different conclusions drawn from various experiments can be attributed to the differing conditions employed in the experimental studies. Thus there is a need for an exhaustive and comprehensive set of experiments to understand the high-field phenomena.

In this paper, we report on high-field stress experiments in gross-defect-free devices. We have done stressing experiments on oxides grown on P-type and N-type silicon, though most have been done on oxides grown on P-type silicon, and we present and discuss mainly the results for this type of capacitors. Oxides grown on N-type silicon showed poorer dielectric integrity because of the inherently higher defect density of these substrates. The basis of our interpretation is the now accepted observation that trap generation occurs in the oxides at high fields. We have done experiments to confirm this observation. The complexity of the trap generation process is also revealed in these experiments. These experiments show that high-field characteristics depend upon bulk point defect generation, interface state generation, and trapping and detrapping in these levels, as well as in as-grown traps. Many of the finer points are explained in the model proposed for the electrical behavior of the MOS capacitor under stress. First we describe our annealing experiment that confirms that hole trap generation and electron trap generation occur during high-field stressing.

The samples used in this study were metal gate MOS capacitors with oxide thickness of 20–40 nm. The substrate was 1 Ω cm (100) P-type Si. The gate oxide was grown in O2 at 950 °C followed by a 20 min anneal in nitrogen at the same temperature. Aluminum evaporation was done in an electron beam evaporation system. Square dots of 1 mm2 were formed by photolithography. The back oxide was etched and aluminum was evaporated for the back contact. Postmetallization anneal was performed at 450 °C for 20 min in nitrogen.

The capacitors were stressed by three techniques: staircase voltage, constant voltage, and constant current. For the constant voltage and constant current stresses, the current through and the voltage across the structure are, respectively, observed as a function of time. For the staircase voltage stress, current measurement has been made after the displacement current decays. Since these are the techniques widely used for high-field stressing, understanding the transients and characteristics for these cases would help give a better model of wear-out with stress time. The configuration used to stress the device consisted of a Keithley 220 current source for constant current stressing with a Keithley 619 electrometer to monitor the voltage, and a Keithley 617 electrometer/voltage source for staircase voltage ampere stressing, as well as for constant voltage stressing. The data acquisition and plotting was done with a HP 9826 computer.
II. RESULTS AND DISCUSSION

In this discussion, capacitors on P-type wafers will be referred to as P-type capacitors and capacitors grown on N-type wafers will be referred to as N-type capacitors. Similarly, the term “stressing in accumulation” will be used if silicon is in accumulation during stressing and “stressing in inversion” when silicon is in inversion.

A. Annealing experiment

MOS capacitors were stressed in accumulation with constant current and HFCV curves were taken before and after stressing. A stress cycle consisted of forcing a current of 0.01 mA/cm² through the capacitor for 100 s. Figure 1(a) shows HFCV curves after stress cycles and an anneal. The HFCV curve after stressing curve (B) not only shows a flatband voltage shift, indicating a positive charge buildup, but also hysteresis on retrace. Furthermore, stretch out in the HFCV curves after stressing indicates the generation of interface states, which drastically increases surface recombination, as confirmed by capacitance transient measurements [Fig. 1(b)]. Fast recovery of the capacitance transient may also be explained by a decrease in the minority carrier lifetime in silicon. But minority carrier lifetime profiling done by the stepped constant capacitance technique showed that high-field stressing affects only the surface generation.

The stressed capacitors were annealed at 200 °C for 10 min. Curve C in Fig. 1(a) shows the HFCV plot after annealing and curve D after a post-anneal stress cycle. It can be seen that the anneal causes the HFCV curve to fully recover to its original position with no hysteresis or stretch out. The capacitance transient also recovers to its original position. The post-anneal stress cycle (curve D) causes a flatband voltage shift $V_{fb}$ significantly larger than after the first stress curve (B). Thus the 200 °C anneal detraps most of the positive charge, anneals most of the interface states and tunneling type of traps near the interface. However, hole traps generated in the bulk are not annealed, as is evident from the larger $V_{fb}$ shift after the post-anneal stress.

Figure 2 gives another evidence of bulk hole trap generation. Curve B in the figure shows the C-V curve after stressing a capacitor with 0.1 mA/cm² for 100 s. Because of interface state generation the HFCV curves show early recovery in inversion. Again, curve C shows that a 200 °C anneal detraps the positive charge, anneals most of the interface states. Curve D shows the CV curve after stress-
ing the capacitor for 100 s with 0.01 mA/cm², which is one-tenth the earlier stress current. However, a larger shift was observed in this case because of the trap generation in the earlier stress cycle. On the other hand, there is not much interface state generation, as seen from little skewing and the nature of HFCV curves in inversion.

In the previous set of experiments, sometimes the second stress did not show net positive charge buildup more than the first stress. The $V$-$t$ transients (Fig. 3) recorded for these samples show that there is a lot of electron trap generation and trapping, including trapping in deeper traps. Although the shallow electron traps detrap in the interval between stressing and CV measurement, sufficient charge remains in the deeper electron traps to partially compensate for the positive charge in the hole traps.

These experiments show that Fowler–Nordheim (F–N) stressing of oxide is a complicated phenomenon in which, besides charge trapping in as-grown traps, there is creation of various kinds of point defects: (i) bulk hole and electron traps, (ii) tunneling type of traps close to the interface, and (iii) interface states. Here we have assumed that positive charge buildup in the oxide indicates bulk hole trap generation in the oxide, and the nonsaturating nature of $V$-$t$ transients indicates electron trap generation in the oxide. These will be elaborated on subsequently.

**B. Stressing studies in accumulation for P-type capacitors**

Current density ($J$) and field ($E$) have been plotted for the F–N characteristics, viz. In $J/E^2$ vs $1/E$, in Fig. 4. For P-type MOS capacitors in accumulation the plot is a reasonably good straight line, which indicates that the current injection is by FN tunneling. Since the semiconductor is in accumulation and the charging effects are negligible $E$ is obtained as $V/t_{ox}$, where $V$ is the voltage across the capacitor and $t_{ox}$ is the thickness of the oxide. This is confirmed by taking IVC measurements at low temperature (Fig. 5). Because of the tunneling mechanism that is virtually temperature independent, the two curves almost coincide; the current at the lower temperature at a particular voltage is a bit smaller because of larger electron trapping at the lower temperature.

For $P$-type capacitors, high-frequency capacitance-voltage (HFCV) curves taken after each stress cycle of constant-current stress showed positive charge buildup in the oxide, for all values of the current. Increase of positive charge in the oxide was observed continuously until breakdown. Similarly, increasing stretchout in the HFCV curves shows that interface states are generated during stressing (Fig. 6). Hysteresis was observed in the HFCV curves after stressing if cycled from accumulation to inversion, or vice versa. The hysteresis was earlier observed by Shatzkes and Av Ron. This hysteresis can be explained by invoking hole or electron traps near the interface that communicate with silicon via tunneling [they could be called tunneling type of traps (TTT), as suggested by Sah].

Voltage transients during constant current stress. While the capacitors were stressed with constant current, voltage transients across them were monitored. Figure 7 shows the
voltage transient under constant-current stress. This shows that voltage increases monotonically until breakdown. The increase in the voltage suggests that the injection field is counteracted by space charge in the oxide. In MOS structures at room temperature this is usually due to trapping of carriers. Since electrons are the majority carriers in the oxide during field injection, the space charge is due to electron trapping mostly in shallow electron traps, which detraps when the stress is removed. Figure 7 shows the voltage transients for repeated stress cycles. The capacitor was stressed for a certain time interval, after which the stress was removed. Stress was restarted after about 10 s. We would like to mention that the period of interruption did not make any qualitative difference in the plots. This figure also shows that the electrons have detrapped at room temperature, since after the interruption transients always begin at a lower voltage than where the previous transient ended.

For P-type capacitors for all values of stress fields, positive charge buildup in the oxide is observed in the HFCV measurements. A plausible explanation is that holes are the majority carriers of the current in the oxide and get trapped, producing nonsaturating voltage transients observed during constant current stressing. However, as we argue below, this is not so.

The idea of tunnel injection of holes from the anode was originally proposed by Weinberg et al. However, their own calculations showed that hole tunneling cannot explain the data. They found that the experimentally determined values of tunneling constants are smaller by three orders from what would be expected for a barrier height of 4.7 eV for holes. The values of tunneling constants calculated from our data for electrons as carriers is quite close to that observed by others and to theoretical estimates. Comparing theoretical models to experimental IVC's at different temperature also suggest that electrons are the majority carriers. Thus, if electrons are the majority carriers injected in the oxide, the increasing voltage transient during constant current stressing implies trapping of electrons. The HFCV's after stress, however, indicate that positive charge is trapped. This discrepancy can be explained by postulating that positive charge buildup occurs to be near the anode and does not alter the cathode field significantly. On the other hand, electron trapping and electron trap generation occur near the cathode (metal in this case), giving rise to monotonic increasing voltage for constant current stressing. Electron trap generation is suggested because of the nonsaturating nature of the voltage transient until breakdown. The positive charge buildup has been observed earlier and has been studied by many workers.

C. Stressing studies in accumulation for N-type capacitors

N-type capacitors stressed in accumulation also showed positive charge generation in the early phase of stressing, but the magnitude of flatband shift was small. Also, this was true only for smaller stress currents. For longer stress times or at very high currents, large stretch-out in the HFCV curve was observed, as shown in Fig. 9. Flatband shifts showed little electron trapping in the oxide. Hysteresis in the HFCV curve was also observed, as shown in the figure, which can be explained by TTT's near the Si SiO₂ interface.

Voltage transients during constant current stress. The voltage transients during constant-current stress for N-type capacitors have been studied in detail for the first time. Figure 10 shows that the voltage decreases until interruption during constant-current stress. The nature of the
curves can be explained as follows. Voltage decrease in constant current stress is due to the positive charge buildup at the Si–SiO₂ interface, which is near the cathode. When the stress is interrupted, some of the holes at the interface detach or tunnel anneal and the cathode field decreases. Thus, after interruption, the voltage increases when stress is started again. Thus these curves can be explained by positive charge buildup at Si–SiO₂ interface. However, the positive charge is not observed in the HFCV curve because positive charge buildup in this case is localized in some areas, and thus does not contribute to flatband shifts. Because of this current confinement, growth of the positive charge remains localized until breakdown. Since silicon is the cathode in this case, electrons get trapped near the Si–SiO₂ interface or recombine with trapped holes, and so the flatband shifts are small.

D. Stressing studies in inversion for P-type capacitors

Usually in high-field studies, stressing in inversion is avoided because of the voltage drop across the depletion layer. However, this is an important mode of stressing, since a MOS transistor is usually operated in inversion, though the inversion charge comes from the source or drain. Stressing in this mode has been studied in detail for the first time. Results are reported here for constant-current stress experiments because the voltage across the depletion layer is taken care of by the current source and wearout data obtained do not depend on silicon properties.

An increase in the positive charge was observed after each stress cycle (Fig. 11). Also, annealing experiments done in this case showed hole trap generation in the oxide. However, for the same stress current and time for constant current stressing, the amount of positive charge observed for this stressing in inversion was less than for stressed in accumulation. This lower positive charge was also observed in the constant-voltage stress, with equal amounts of charge passed through the oxide. These observations show that either positive charge buildup is less in this case because of the basic mechanism of positive charge generation or that along with the positive charge buildup, electrons also get trapped or neutralize trapped holes. That electron trapping seems to be the cause is evident from the voltage transients observed during constant-current stress. This is described later in the discussion on voltage transients.

The hysteresis that is observed after stressing in accumulation experiments was also observed when the capacitor was stressed in inversion. However, the direction of hysteresis was, in this case, opposite to that observed for P-type capacitors stressed in accumulation for the early phase of stress. If the stress continues, then the direction of hysteresis reverses and becomes the same as observed for the capacitors in accumulation (Fig. 11).

In this case (stressing in inversion for P-type) hysteresis can be explained by invoking electron TTT near the metal or due to mobile ions such as hydrogen. For longer stress cycles the direction of hysteresis changes because TTT's are generated continuously at the Si–SiO₂ interface, and eventually the effect of these traps dominates the HFCV curve.

Voltage transients during constant current stress. For P-type capacitors stressed in inversion the V-t curves were noisy and the voltage required for the constant current was much higher than in accumulation (Fig. 12). This observation was also made in earlier studies.\(^1\)\(^7\) This is due to the large generation lifetime of the carriers in the substrate.
The voltage transients increase with time suggesting there is electron trap generation and trapping near the cathode, or possibly a negative charge in interface states. Actually this stressing condition is similar to stressing \(N\)-type capacitor in accumulation i.e., silicon acts as a cathode, and one would expect localized positive charge buildup. But as Fig. 12 shows that such localization of positive charge and current confinement was not observed when \(P\)-type capacitors are stressed in inversion. This can be explained as follows. In the case of \(P\)-type capacitors stressed in inversion, electrons coming from the depletion region are hot, and their injection into the oxide is not influenced too much by the localized fields at the interface. Furthermore, the depletion layer space charge in the semiconductor masks the effect of charge trapped in the oxide and does not allow positive feedback, leading to current confinement.

**E. Stressing studies in inversion for \(N\)-type capacitors**

If \(N\)-type capacitors are stressed in inversion, along with the positive charge buildup, stretchout, and hysteresis are also observed in the HFCV curves. The direction of hysteresis is the same for all stress cycles and the same as observed for \(N\)-type capacitors in accumulation (Fig. 13). This can be explained by the generation of TTT's near the Si–SiO\(_2\) interface.

*Voltage transients during constant current stress.* In the constant-current stress experiment, the voltage increases until interruption for all stressing cycles (Fig. 14). This indicates electron trapping near the Al–SiO\(_2\) interface. The figure also shows the detrapping of electrons during interruption of the stress. Thus these curves can be explained by invoking electron trapping and detrapping near the metal–SiO\(_2\) interface.

**F. Stressing experiments with polarity reversal**

In these studies capacitors were stressed alternately in accumulation and inversion. These studies were done mostly using constant-current stress, because the field across the oxide remains about the same for both polarities and it is easier to track and control charge through the oxide.

\(P\)-type capacitors when stressed in either inversion or in accumulation show positive charge buildup in the oxide. Now if the polarity of stressing is reversed, reduction of the positive charge is observed, as shown in Figs. 15 and 16 for both kinds of polarity reversals (i.e., either stressing in accumulation followed by inversion or in inversion followed by accumulation). If the oxide is stressed further after reversal, positive charge growth is again observed. In many cases, particularly for high current stressing, the oxide would break down immediately after the polarity change. This is because of the sharp rise in the cathode field after polarity change.

Figure 17 shows the observations for \(N\)-type capacitors. If the oxide is stressed initially in accumulation, the HFCV curve shows interface-state generation and electron trapping. Now, if the polarity of stressing is reversed then more interface states are generated, but now positive charge buildup is observed in the HFCV curves. If stressing is continued in inversion then positive charge and stretchout both increase, but if the polarity is again reversed, then negative charge trapping is observed. This also indicates that holes trapped in inversion stressing get tun-
nel annealed or recombine with electrons. The nature of observations was also the same if the initial stressing was done in inversion. This shows that electron trapping near the cathode and hole trapping near the anode are taking place.

III. PHENOMENOLOGICAL MODEL

Based on these observations a comprehensive model for the electrical behavior of MOS capacitors under stress is proposed. According to this model the electrical characteristics of MOS capacitors at high fields can be explained considering the following points.

(i) Current through a MOS capacitor at high fields is primarily due to electrons tunneling from the cathode by the Fowler–Nordheim mechanism.

(ii) Electron and hole traps are generated during the stressing: along with the bulk electron and hole traps, tunneling type traps (TTT), as well as interface states are also generated during the stressing.

(iii) There is always positive charge generation near the Si–SiO₂ interface for all structures and stress conditions.

(iv) Electrons are trapped near the cathode and holes are trapped near the anode in as-grown and stress generated traps.

(v) Some of the traps are shallow in energy and carriers may detrapping at room temperature.

(vi) Silicon, especially good quality silicon, is a poor injector of carriers in inversion.

(vii) Electron and hole trapping may be localized spatially.

Some of these processes may occur simultaneously in the capacitor. The electrical characteristics then depend upon the combined effect of these processes. For example, we do not see net positive charge buildup while stressing N-type capacitors in accumulation, because in this case silicon is the cathode and thus the HFCV curve shows the combined effect of the positive charge buildup and the electron trapping or recombination with trapped holes.

The above observations are for stress fields below breakdown fields. However, these observations tell us about the events leading to breakdown and thereby about the breakdown mechanism. The final stages of breakdown are discussed in the next section.

IV. BREAKDOWN OF MOS OXIDES

Physical processes are less understood in amorphous insulators than in crystalline insulators or semiconductors and this is applicable to dielectric breakdown also. In spite of extensive experimentation and theoretical investigation in the last 25 years, the mechanism of dielectric breakdown
has remained poorly understood. In this paper, we present experiments on dielectric breakdown, which might help understand the final stages of breakdown.

Breakdown in SiO₂ has been classified into three categories: defect-related breakdown, dielectric wear-out, and intrinsic breakdown.

However, the distinction between these terms is not clear, at least for MOS oxides. According to Shatzkes and Av Ron, defect-related breakdown and wear-out cannot be distinguished. Wolters et al. suggested that defect-related breakdown and intrinsic breakdown phenomena are the same. There however, is a consensus that breakdown in MOS oxides is electronic and three electronic processes, which finally lead to breakdown, are suggested to be operative, which finally lead to breakdown.

1. The oxide erodes near the charge trapping centers and then there is low resistance channel from cathode to anode.

2. The number of traps increases to a large number, and finally this leads to a leakage path through processes-like resonant tunneling, and finally oxide breakdown.

3. The positive charge at the anode grows toward the cathode and finally the oxide breaks down because of increased cathode field.

We will discuss the observations related to breakdown for P-type and N-type capacitors in accumulation and inversion. Thus the model presented here considers all these cases separately. This comprehensive approach has been taken for the first time.

A. Breakdown of P-type capacitors

While studying breakdown of P-type capacitors in accumulation at different fields, an important observation for breakdown was that two mechanisms appeared to be operating in different ranges of fields. At high fields, the oxide breaks down because of regenerative positive charge buildup. At low fields, the oxide may break because of trap generation and increase of current due to resonant tunneling.

There is some experimental evidence for this in the literature also. Wolters et al. observed that when capacitors are stressed with constant current in accumulation, the charge to breakdown $Q_{bd}$ remains constant over the wafer. However, they found that the oxide breaks down with different values of $Q_{bd}$ in two current ranges: one below a particular value $J_{cr}$ (this was about 1 mA/cm²) and the other above this value. For very high values of currents ($J>J_{cr}$), the oxide breaks down with a very low value of $Q_{bd}$. We have shown that this is observed in the case of constant voltage stress also. At high fields (above about 11.5 MV/cm), $Q_{bd}$'s were very low. The value of $Q_{bd}$ below field 11.5 MV/cm was 1 C/cm²; above 11.5 MV/cm it was $1 \times 10^{-3}$ C/cm². The volt ampere cycling experiments clearly show different natures in the different range of fields, and we discuss this below.

The HFCV curves obtained after repeated volt ampere or constant-voltage or constant-current stressing invariably show positive charge buildup. $I-V$ characteristics are different in subsequent volt ampere cycles. After interruption, the next $I-V$ curve depend upon the range of voltages applied previously. For low values of voltage (such that the oxide fields is below 10 MV/cm), the current would decrease in subsequent cycles for the same values of voltage and the oxide would break after many cycles. These characteristics are shown in Fig. 18. This indicates electron trapping. However, the HFCV plots show the presence of positive charge in the oxide. This suggests that electron trapping in the bulk and near the cathode dominate the injection process, while positive charge buildup near the Si-SiO₂ interface dominates the HFCV's.

At high fields, however, repeated IVC's show an increase of current for all values of voltage for repeated stress cycles (Fig. 19). This shows that at such high fields the positive charge generation rate is quite high and annuls the effect of electron trapping. Hence the current increases due to increasing the cathode field. When the positive charge exceeds a certain amount, the oxide breaks down.

In the intermediate field range, the repeated $I-V$ characteristics did not have any definite trend (Fig. 20). This indicates that traps generated in the bulk are of both types and the characteristics are determined by the dynamics of trap generation and charge trapping and detrapping.
Thus the breakdown mechanism in this case can be explained as follows. At high fields, oxide breaks down because of regenerative positive charge buildup. This positive charge buildup is due to hole trap generation and subsequent trapping. At low fields oxide may break because of electron and hole trap generation and increase of current due to resonant tunnelling. Since both types of carriers get trapped near their respective electrodes there is no field enhancement that increases the current. Breakdown eventually occurs due to leakage paths caused by the traps. In the intermediate range and any one of these processes might dominate. However, it should be noted that trap generation in the oxide plays an important role in the eventual breakdown.

When P-type capacitors were stressed in inversion with constant current or constant voltage, there were many early breakdown events. This could be because of two reasons: the early breakdowns could be due to collapse of the deep depletion region due to formation of microplasmas and consequently increased field in the oxide. Also, since silicon is the cathode, and at high field, positive charge builds up at the Si–SiO₂ interface. This positive charge enhances the cathode field further, and this regenerative process is responsible for the breakdown.

Capacitors that do not show early breakdown have low hole trap density and very good quality silicon substrate. They survive because the initial positive charge buildup is not fast enough to increase the cathode field to a high enough value. Electron trapping starts and this counteracts the positive charge buildup and neither is there the problem of depletion layer collapse. As stressing continues positive charge at the interface increases, as is evident from HFCV curves. The oxide breaks either after a certain amount of the positive charge buildup, which causes enhancement of the cathode field or because trap generation in the oxide exceeds the density required to provide a continuous leakage path through the oxide.

**B. Breakdown of N-type capacitors**

When N-type capacitors are stressed in accumulation, oxide breakdown is mainly determined by the positive charge buildup in arccally localized spots. The process is regenerative and is observed in all ranges (Fig. 10). The regenerative positive charge buildup is localized phenomenon and discussed in Sec. II C. Breakdown in this case is mainly decided by the rate of positive charge buildup, rather than any other mechanism.

When N-type capacitors are stressed in inversion, electrons are injected from metal and effects are similar to stressing of P-type capacitors in accumulation. HFCV curves after stress show positive charge buildup and the voltage transient in constant-current stress shows negative charge buildup during stressing. The mechanism of breakdown is also similar to that of P-type capacitors in accumulation.

**V. CONCLUSION**

Bulk trap generation and interface state generation due to high-field stressing are the major observations in this study. The observation that in all the above experiments we have not seen positive flatband shifts in the C–V curves (corresponding to net negative charge buildup in the oxide) indicates that at the Si–SiO₂ interface there is always hole trap generation and hole trapping that affect the HFCV. We have proposed a model that describes various electronic processes that occur at high fields. The combined effects of these processes explains most of the high-field characteristics, observed by us as well, as reported in the literature.

During high-field stressing, processes like trap generation, trapping, and detrapping occur simultaneously. High-field characteristics can be explained on the basis of these processes. Another important observation is that positive charge buildup at the Si–SiO₂ interface or near the anode may enhance the cathode field, leading to breakdown. This positive charge buildup plays an important role in the degradation of dielectric qualities and the breakdown mechanism of the oxide.

However, the microscopic nature of the positive charge is not yet clearly identified. As reported by Wolters and Hokari, positive charge in the oxide cannot be explained only by hole trapping in existing traps. It has been suggested that two distinct species of positive charge can be generated near the Si–SiO₂ interface. These species are the trapped holes and anomalous positive charge (or APC). Our annealing experiments and hysteresis do suggest that there definitely is hole trap generation and subsequently hole trapping, which contribute to positive charge observed in the oxide. This positive charge buildup near Si–SiO₂ interface plays an important role in the wear-out mechanism, and can be used to estimate the reliability of the oxide.

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3D. R. Wolters J. J. Van Der Schoot, and T. Foorer in Ref. 1, p. 56.


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