Abstract—Current transformers form an integral part of protective systems. Ideal Current Transformers (CTs) are expected to reproduce the primary current faithfully on the secondary side. Often, during fault conditions an important component of current is exponentially decaying DC offset current. Under such conditions the CT saturates, and hence it cannot reproduce the primary current faithfully. This paper deals with experimental methods for determining CT performance under saturation. A laboratory setup has been developed to observe CT response under steady state and fault conditions. Thus, it is now possible to experimentally evaluate the CT performance under fault conditions.

Index Terms—CT Saturation, Power System Protection, Education.

I. INTRODUCTION

The faithful replication of fault current is an important requirement in relaying. Unless Current Transformer (CT) secondary replicates faithfully the fault current, relay’s decision cannot be considered dependable, secure and accurate. This is particularly true for distance relaying or differential relaying schemes. For example, due to CT saturation, a distance relay may fail to detect the fault (lack of dependability) and a bus differential relay may operate on the external fault (lack of security). Thus, the relay should operate before the onset of CT saturation.

This enforces stringent requirements on speed of relay. A distance relaying is expected to operate within 1-cycle (before onset of CT saturation) and bus differential numerical relay in a quarter of cycle [1].

Study of literature on CT [2], [3] shows that the performance of CT is not experimentally evaluated at all for representative fault current signals. Reasons for this observation can be followings:

1) A fault has both sinusoidal AC component and DC offset component. While it is possible to generate AC current source, generation of composite current signal is a non-trivial task.

2) Relay test benches are designed to test dynamic performance of relay. They can generate scale down replica of actual fault current signals using Electro Magnetic Transient Program (EMTP). Power amplifiers are used to amplify current signal to the level required by the relay. Since the corresponding current levels are much below the CT primary fault current level, relay test bench can not be used to excite CT. Hence, relay test benches cannot be used for CT testing.

Therefore, we conclude that performance of CT is not evaluated at all for the representative fault current.

This paper, for the first time, proposes experimental methods to do such testing. Also, it is our experience that students find it difficult to appreciate the reasons and consequences of CT saturation on performance of protection system. It is difficult to demonstrate the consequences of CT saturation to the students in a laboratory setup for the simple reason that it is difficult to simulate the fault current in laboratory setup. Thus, our motivation for this work is also from an educational perspective. This gives a tutorial flavor to the work.

In this paper, we will design simple and innovative circuits to synthesize fault current waveforms by superposing an AC current source and DC offset current source in the primary of CT. The DC offset current source can be developed by two approaches, 1) Simple R-L and 2) R-C circuits. Superiority of R-C based DC offset current source over R-L circuit based current source will also be demonstrated.

This paper is organized as follows. In section-II, reasons for CT saturation are explained. In section-III, analysis of CT saturation under AC excitation is carried out. This is followed by analysis of CT saturation under influence of DC offset current. In section-IV, experimental setups with the results are presented. Section-V concludes the paper.
II. REASONS FOR CT SATURATION

Nature of Fault Current

Consider an AC source, which feeds a load through a transmission line. The single line diagram is as shown in Fig.1. The transmission line parameters \( R_{\text{line}} \) and \( L_{\text{line}} \) are shown as lumped. When the switch \( S \) is closed, it represents the existence of a fault. The fault current as seen by the current transformer primary winding is shown in Fig. 2.

Let the voltage source be represented as follows:

\[
V(t) = V_m \sin(\omega t + \theta)
\]

For simplicity, assume that fault strikes at \( t = 0 \).

Fig. 2. Fault current waveform

Then, the instantaneous value of the fault current for \( t \geq 0 \) is given as,

\[
i(t) = \frac{V_m}{|Z|} \sin(\omega t + \Psi) - \frac{V_m}{|Z|} \sin(\theta - \Psi) e^{-\frac{R_{\text{line}}}{L_{\text{line}}} t}
\]

In equation (1), \( R_{\text{line}} \) and \( L_{\text{line}} \) are the transmission line resistance and inductance, \( |Z| \) is the impedance of the transmission line and \( \Psi \) is the impedance angle of transmission line. We assume no load as pre-fault condition.

If \( \theta - \Psi = \pm 90^\circ \), then the magnitude of DC offset is maximum. When, \( \theta - \Psi = 90^\circ \), the fault current is given by,

\[
i(t) = \frac{V_m}{|Z|} \sin(\omega t + \pi/2) - \frac{V_m}{|Z|} e^{-\frac{R_{\text{line}}}{L_{\text{line}}} t} \]

and, \( i(t) = 0 \), at \( t \leq 0 \)

In equation (2), as time \( t \) approaches infinity (\( t \to \infty \)), the DC component term reduces to zero [4].

III. ANALYSIS OF CT SATURATION

A. Saturation due to AC Current

The rms value of emf generated across the secondary of the CT is given by [5],

\[
E_s = 4.44f\Phi_m N_s
\]

\( \phi_m \) is the maximum flux linking with the secondary, \( \omega \) is supply frequency, and \( N_s \) is the number of turns on secondary side. If the CT leakage inductance is neglected and CT burden is considered purely resistive then,

\[
E_s = (R_s + R_b) I_s
\]

Where, \( R_s \) and \( R_b \) are secondary resistance and secondary burden.

Due to the occurrence of a fault, the secondary current \( (I_s) \) increases. As a result of this, \( E_s \) also increases and so does \( \phi_m \). When \( \phi_m \) crosses the knee point, the CT starts saturating. Therefore, the magnetizing impedance of the CT reduces, resulting in an increase in the magnetizing current.

Thus,

\[
\frac{\Phi_m}{I_s} = \frac{N_p}{N_s}
\]

In fact, during saturation instantaneous secondary voltage is zero \( (e_s = 0) \) and thus for a resistive burden, clipping of current waveform takes place. Thus, an increase in flux above the knee point can cripple the output of the current transformer. When the instantaneous flux reduces below the knee point, CT comes out of saturation and the primary current is properly replicated. Protection grade CTs are generally designed to faithfully reproduce to sinusoidal currents up to 20 times the rated value, provided the CT burden is kept sufficiently low [2]. However, lead impedance, relay impedance and burden imposed by magnetizing current of other phase CTs during unbalanced fault e.g. single line to ground fault can all contribute to large CT burden and this can lead to saturation under sinusoidal AC currents.

B. Saturation due to DC Offset Current

From equation (1), DC offset current is given by

\[
i_{dc} (t) = I_0 e^{-\frac{R_{\text{line}}}{L_{\text{line}}} t} \quad \text{When } t \geq 0
\]

Otherwise, \( i_{dc} (t) = 0 \)

Therefore, assuming purely resistive burden, the voltage across the CT secondary due to DC offset current is given by,

\[
e_s(t) = \frac{N_p}{N_s} (R_x + R_b) I_0 e^{-\frac{R_{\text{line}}}{L_{\text{line}}} t}
\]

Also, \( e_s(t) = N_s \frac{d\phi}{dt} \)

Integrating equation (3) and (4) with respect to \( t \), from limits ‘0’ to ‘t’, we get,

\[
\phi_{dc}(t) = (1-e^{-\frac{R_{\text{line}}}{L_{\text{line}}} t}) \left[ \frac{N_p I_0}{N_s^2} \left( \frac{L_{\text{line}}}{R_{\text{line}}} \right) (R_x + R_b) + \phi_0 \right]
\]
φ₀ is the initial value of flux, for simplicity we assume φ₀ = 0. This accumulation of DC flux is as shown in Fig. 3.

Prior to fault, it is seen that DC flux is zero and it increases to its steady state value. Further, unlike AC flux its average value is not zero. Now, the total flux present in the CT is as follows:

\[ \phi(t) = \phi_{dc}(t) + \phi_{ac}(t) \]  \hspace{1cm} (6)

Fig. 3. Plot of DC flux with respect to time

Fig. 4. Superimposition of the AC flux over the DC flux

The superimposed AC and DC flux wave can be represented as shown in Fig. 4. Consequence of DC flux is that instantaneous flux may increase beyond design value. This can saturate a CT and cause clipping of the secondary current.

IV. EXPERIMENTAL SETUP

A. CT Calibration and AC Saturation

The CT used in our study is a class T (used for differential protection) 15 / 5Amp [2]. The CT primary circuit is connected to a constant AC current source. It consists of a single-phase autotransformer connected to a step down transformer. The autotransformer is used to set the magnitude of current. The step down transformer provides scaling or amplification of current.

When the secondary of CT is short-circuited, \( I_p \) versus \( I_s \) of CT shows a linear response. To evaluate CT performance under load, a burden of 4.5Ω is introduced in the secondary circuit. Different sets of primary and secondary currents are recorded from zero to rated primary value by adjusting the value of primary current source. The above procedure is repeated for different values of load on the CT secondary (in this case, the burden is 4.5Ω and 18Ω). The characteristics obtained are as shown in Fig. 5. It can be seen from the figure, increase in burden saturates the CT rapidly. Thus, as the secondary burden increases, the problem of saturation becomes more and more pronounced.

Fig. 5. CT calibration curve with burden of 4.5Ω and 18Ω

The instantaneous secondary current waveform with CT burden of 9.5Ω is shown in Fig. 6. It is seen that there is a significant clipping of CT secondary current when primary AC current faces a large secondary burden. In the next section we illustrate CT saturation on DC offset current.

Fig. 6. Secondary current waveform across CT secondary for burden of 9.5Ω.
B. CT Performance on DC Offset Current only

Fig. 7 shows the experimental setup for evaluating CT performance under DC offset condition. DC offset current is obtained by energizing a large inductor with current and then releasing this high energy in the form of DC offset current in the CT primary circuit. Resistance $R_2$ can control the magnitude of inductor current.

Fig. 7. Setup for obtaining pure DC offset in CT secondary

Initially, when the single pole switch $S-1$ is closed, the reverse blocking of diode allows only charging of inductors and it does not allow any DC current through the Current Transformer.

Fig. 8. Exponential Decay of current across primary of CT

However, when the DC source is isolated (switch $S-1$ open), the energy stored in the inductor is dissipated through primary winding of CT and the power diode. The diode now is forward biased thus providing a discharge path through the primary of CT for current to decay exponentially. This arrangement is used to generate the decaying DC component. The digital storage oscilloscope is connected across the secondary terminals of the CT and an external trigger is provided to the digital storage oscilloscope to capture the waveforms at the moment DC is injected in the secondary circuit.

Fig. 9. Exponential Decay of current through the secondary of current transformer

The waveforms obtained at the time of discharging across the primary and secondary are as shown in Fig. 8 and 9 respectively. It is seen that CT can faithfully replicate the DC offset current if it does not saturate. For this purpose, as in this experiment, burden on the secondary side should be kept sufficiently low.

C. Synthesizing the Typical Fault Current

The next set of experiments aim to synthesize the fault current by adding DC offset current to the primary AC current. CT is operated under normal conditions by exciting the primary with a constant AC current source. A small burden is connected in the secondary circuit. We now discuss two methods of superposing DC offset current on sinusoidal AC current to generate a composite signal indicative of fault current.

1. Method-I Using R-L Circuit

Fig. 10 illustrates the experimental setup. Sinusoidal component of the fault current is injected into primary winding of CT by current source $I_{ac}$. To obtain DC offset component of the fault current, an inductor L is charged by closing switch $S-1$. A battery set is used to provide the DC voltage and resistance $R_1$ limits the inductor current. As the switch $S-2$ is in OFF position, the DC and AC circuits are completely isolated. To create the DC offset current, the $S-2$ is switched ON and $S-1$ is switched OFF, thereby discharging the stored magnetic energy through the diode in to the primary winding of current transformer. Resistance $R_2$ is used to control the time constant during discharging. The diode blocks the interaction of the DC source with the primary winding of the CT.

Effect of CT saturation on the secondary current is seen in the Fig. 11. The similarity of the waveform to what has been observed in the field is obvious [5], [6]. The current waveform is stored in the digital storage oscilloscope. It can now be concluded that, it is possible to evaluate the performance of CT under fault condition in the laboratory.

Fig. 10. Setup for synthesizing fault current, using R-L circuit

A complicating factor of the circuit shown in Fig. 10 is that of switching requires, simultaneous opening of switch $S-1$ and closing of $S-2$, which is difficult to realize. This leads to
arcing across the switch. Method-II, to be discussed now, overcomes this problem by using R-C circuit.

2. Method-II Using R-C Circuit

Experimental setup is as shown in Fig. 12. This is a much simpler circuit, as it does not involve any arcing across the switch poles. When switch $S$ is in position 1, Capacitor $C$ is charged through $R_1$ and $R_2$. Series resistance $R_1$ is used to limit the charging current. When switch $S$ is in position 2, a variable resistance $R_2$ is used to obtain the desired time constant. In our experiment the value of capacitor $C$ and $R_2$ was selected to get a time constant of the order of 180 ms.

![Fig. 12. Setup for simulating saturation in CT both by AC and DC currents combined, using R-C circuit](image-url)

In Fig. 12, AC current source would interfere with R-C circuit, when switch $S$ move to position 2. Also from an AC current source perspective, current has to split between two parallel paths provided by CT primary and R-C network. CT burden was about 18Ω. To minimize the leakage effect, large $R$ and $C$ values are selected so that AC current predominantly flows through the CT primary circuit. Fig. 13 illustrates the CT saturation current waveform. As can be seen, current clipping due to the saturation effect in CT can be observed using R-C circuit also. The results are much better compared to method-I, as the arcing across the switch in method-I is totally eliminated.

![Fig. 13. Saturation curve across CT secondary, using R-C network.](image-url)

V. CONCLUSIONS

Experimental evaluation of CT performance requires replica of fault current in the CT primary winding. Such a large current can not be generated by a relay test bench. Therefore in this work, we have reported an experimental (laboratory) setup, which has been used to evaluate the performance of CT under:

1. Large AC currents (indicative of steady state fault current) and
2. Exponentially decaying DC offset current (indicative of transient component)
3. Composite current signals made up of components 1 and 2 that mimic the fault.

For this purpose, an AC current source and an exponentially decaying DC offset current source have been designed and developed. By using R-L and R-C circuits, it was shown that, we can inject the DC offset current component into primary winding of CT. It was shown that R-C circuit is more effective than R-L circuit in synthesizing the fault current waveforms. The results are consistent with the expected CT behavior.

Authors are not aware of any previous work, which demonstrates experimental evaluation of CT performance under fault like current signals. Thus, by using the proposed method, it is possible for relay engineers to test the CT with nearly exact fault current signals.

VI. REFERENCES


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