A Low-Power and Compact Analog CMOS Processing Chip for Portable ECG Recorders

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Abstract—This paper presents a three-channel low-power and compact analog processor including a test chip, fabricated in TSMC 0.35µ mixed-mode CMOS process, for portable Electrocardiogram (ECG) monitoring devices. The chip highlights integrating CMOS instrumentation amplifiers based on current balancing technique to implement more analog signal conditioning functions at instrumentation amplifiers. First order low-pass filtering as well as programmable high-pass filtering has been included in each instrumentation amplifier. Experimental results show that each channel draws 22µA from a 3.3V battery. Measurement results satisfy recommended specifications for portable ECG recorders. The programmable test board, designed using the chip, records three-leads ECG with frontal plane and precordial leads. Analog signal conditioning circuit, measurement results and recorded ECGs are given in this paper.

I. INTRODUCTION

Low power supply consumption, weight and cost are important issues in personal biomedical instruments. The performance of any personal biomedical system depends on the performance of analog signal conditioning, e.g. extraction and amplification of low-level biopotential signals with maximum amplitude of a few mV from a noisy environment mainly by using instrumentation amplifiers and then gain and filter stages. To reduce the cost and weight as well as the power compact design of personal medical instruments is desired. The current balancing technique is a low-cost approach for designing instrumentation amplifiers [1,2,3]. Current-balancing technique enables the designer to include more functionality in the instrumentation amplifier and hence next analog stages will be simpler. In this paper a three-channel low power analog CMOS processing circuit for personal ECG monitoring applications and developed test board are presented. The circuit uses a test chip, which was fabricated in TSMC 0.35µ mixed-signal CMOS process. Ultra low power biopotential instrumentation amplifiers based on current balancing technique and programmable high pass filtering, low power operational amplifiers (op-amp) and wide-swing bias circuit have been designed and implemented on the test chip. Other analog processor integrated circuits have been reported already [4, 5]. The distinguishing features of the presented design as compared to earlier works are using CMOS instrumentation amplifiers based on current balancing technique for ECG signal conditioning, its low power consumption, compact design and programmable high-pass filter included in the instrumentation amplifiers. The latter is used selectively for base line drift compensation. Circuit description of the chip modules, test board, measurement results and recorded ECGs are given in this paper. The test board is programmable in such a way three-leads ECG including frontal plane and precordial leads are selectively recorded.

II. TEST CHIP MODULES

The test chip was designed with independent low-power functional modules operating with battery supply voltage ranging from 3V to 4V. Low frequency band of biosignals enabled us to keep the connection among the modules off-chip. In this way we were able to characterize each module separately as well as implementing and testing of different analog signal conditioning circuits. The chip consists of three ultra low-power current-balancing instrumentation amplifiers with digitally programmable high pass filtering and provision for low-pass filtering, six low-power op-amps and low-power wide swing bias generator as shown in Fig. 1.

A. Instrumentation Amplifiers

Monolithic implementation of instrumentation amplifier by using traditional three op-amp configuration needs accurate matching of the resistors used in its feedback network to achieve high CMRR. Also this structure is not a proper solution for very low power design.

Another approach for design of instrumentation amplifiers is to use current-balancing technique [3]. Fig. 2 shows the schematic of each current balancing instrumentation amplifier implemented on the chip. At the transconductance stage, the input difference voltage is converted into a differential current $i_g$ flowing across resistor $R_g$. Current $i_g$ is mirrored to the transimpedance section with
unity gain. The mirror current, called i_m, is converted into
modules. Low-power two-stage op-amps with push-pull
B.
external capacitors at the input of instrumentation amplifier.
normal level internal switch S2 is used for fast discharging of
signal conditioning modules. To return the base line to the
rapid variation of half-cell potential may saturate the ECG
load capacitor of 40pF was considered for op-amps to be
medium gain and low-frequency applications. Maximum
very low bias current guess [1].

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Instrumentation amplifiers were designed by an iterative
limit the gain of instrumentation amplifier to six.
was used to implement Rg and Rs. This constraint led to

\[
\frac{V_{out} - V_{ref}}{V_{in+} - V_{in-}} = \frac{R_s}{R_g}
\]

Cascode current mirror was used in the instrumentation
amplifiers to obtain high CMRR [3]. We decided to use on-
chip resistors Rg and Rs to have less external components. Two external capacitors CHPF and CLPF determine the lower and higher cutoff frequency of the amplifier, respectivly. We made the high-pass filter action to be
programmable by using two external control bit lines and if
necessary bypass it as shown in Fig. 2.

The main concern in the design was to fabricate very
low-power instrumentation amplifiers while their main
 specifications satisfy requirements of analog front-end
modules for portable personal biomedical instruments
especially for personal ECG monitors [1,6]. To do this, the
target CMRR was taken to be at least 90dB, maximum input
referred noise voltage to be less than 10µV RMS in 200Hz
BW and minimum input voltage dynamic range to be ±5mV.
Resistors of high sheet resistance were not available in the
cconcerned fabrication process. Hence the P⁺ implant layer
was used to implement Rg and Rs. This constraint led to
limit the gain of instrumentation amplifier to six.
Instrumentation amplifiers were designed by an iterative
power-oriented design procedure, starting from an initial
very low bias current guess [1].

Sudden changes in the base line due to quick motions and
rapid variation of half-cell potential may saturate the ECG
signal conditioning modules. To return the base line to the
normal level internal switch S2 is used for fast discharging of
external capacitors at the input of instrumentation amplifier.

B. Operational Amplifiers and Bias Circuit

Power was also the main concern in the design of other
modules. Low-power two-stage op-amps with push-pull
output stages were designed. Op-amps were sized for
medium gain and low-frequency applications. Maximum
load capacitor of 40pF was considered for op-amps to be
able to connect the output of op-amps directly to data
converters used for signal digitization. Since the
instrumentation amplifiers include first order bandpass
filtering it’s enough to use simple first-order active low pass
filtering following the instrumentation amplifier for each ECG
channel.

The low-power wide-swing cascode beta multiplier was
realized to provide bias currents for all modules on the chip.
To avoid any extra current dissipation the cascode current
mirrors of the instrumentation amplifiers were sized such
that their bias voltage can be taken from available voltages
from cascode beta multiplier used for bias generation.

III. COMPACT ANALOG SIGNAL CONDITIONING

If the ECG signal is to be preserved then the analog front
end of the ECG recorder must have the appropriate
frequency characteristics, noise and dynamic range. On the
other hand integrating signal conditioning functions at
instrumentation amplifier module reduces complexity and
power of the whole analog processing circuit. Hence by
using ultra low-power implemented instrumentation
amplifiers having gain and bandpass frequency response and
considering performance parameters according to the
recommendations for ECG recorders a compact analog
signal conditioning circuit was developed for each channel of
ECG recorder as shown in Fig. 3.a. This circuit draws
average current of 22µA from 3.3V battery supply voltage.
The front-end differential stage is AC-coupled via capacitors
C1 and C2 with bias resistors R1 and R2. The overall gain
of the channel was set at 200 using internal op-amps and 600
using off-chip low-power op-amps. The cut-off frequency of
internal HPF is programmed by using two control bits and
one external capacitor. For example for external capacitor of
1µF the cutoff frequency is programmed from 0.05Hz to
0.07Hz. Corner frequency of low-pass filtering achieved in
the instrumentation amplifier and second gain stage were set
to 170Hz.

IV. MEASUREMENT RESULTS

Fig. 3.b shows the test chip photo. It was implemented in
0.35µ TSMC mixed-mode CMOS process through MOSIS
service. The chip area was pad limited because of using test
pads and external connection of chip modules. Each
instrumentation amplifier and op-amp occupies 0.2mm² and
0.08mm² area, respectively. Measurement results show that
each op-amp and bias generator draws 8µA and 10.5µA dc
current from 3.3V battery supply voltage, respectively. Op-
amps have phase margin of 70 degree while driving 40F
load capacitors. Unity gain frequency of the op-amps was
measured 130KHz suited for low-frequency biopotential
signals.

Instrumentation amplifiers are the main building blocks
on the chip and highlight the main performance parameters
of the analog signal conditioning for each ECG channel.
Table I shows the implemented channel specifications.

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Figure 2. Schematic diagram of each low-power instrumentation amplifier on the chip

Figure 3. (a) Low-power compact analog signal conditioning circuit for each ECG channel (b) Fabricated test chip photo
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain of the channel</td>
<td>600</td>
</tr>
<tr>
<td>Average supply current for each channel</td>
<td>22µA</td>
</tr>
<tr>
<td>Input voltage dynamic range</td>
<td>± 6 mV</td>
</tr>
<tr>
<td>CMRR</td>
<td>100dB (60Hz)</td>
</tr>
<tr>
<td>Input common-mode voltage range</td>
<td>0.3V &lt; CMR CMR &lt; Vdd-1V</td>
</tr>
<tr>
<td>HPF cut off frequency</td>
<td>0.05Hz (Programmable)</td>
</tr>
<tr>
<td>LPF cut off frequency</td>
<td>170Hz</td>
</tr>
</tbody>
</table>

V. EXPERIMENTAL ECG RECORDING

Application board of the test chip was designed and used to record three ECG channels. It was decided to have a programmable scheme in such a way three frontal plane leads as well as precordial (chest) leads are recorded. To be able to record precordial leads Wilson central terminal circuit is required. This terminal provides reference potential for measuring precordial leads [6]. Since on chip op-amps were not low-noise Wilson central terminal circuit was implemented by using OPA4336 quad op-amp, which is a low-power low-noise op-amp available from Texas Instrument. Fig. 5 shows the test board with test chip mounted on a general-purpose PCB lambda for LQFP packages.

Once the ECG signal has been amplified and filtered, it must be digitized. We used a ready-made interface circuit already developed in our department. This interface circuit uses microcontroller MSP430F149 from Texas Instruments to digitize the analog biopotential signals. MSP430F149 has internal 12-bit ADCs (Analog to Digital Converters). The interface circuit uses a GUI (Graphic User Interface) already developed by Visual Basic language in our department, to show the recorded ECGs.

The application board of the test chip was used to record ECGs. Fig. 5 shows recorded lead II-ECG and lead V5-ECG belonging to frontal plane leads and precordial leads, respectively. Since the interface circuit was able to display one channel at a time the presented ECGs are not concurrent.

VI. CONCLUSIONS

A single supply battery-operated ultra low power analog test chip, intended for three-leads ECG signal processing is presented in this paper. This chip draws 66µA from a 3.3V Lithium-ion battery when all channels are enabled. Integrating signal conditioning functions at instrumentation amplifier module reduces complexity of the next stages.

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