ABSTRACT
Endurance and retention of SONOS EEPROMs operated using channel hot electron injection (CHEI) and band-to-band tunneling (BTBT) induced hot hole injection (HHI) are studied. Cycling window closure is improved by optimizing erase bias, and its effect on cell degradation is studied. The retention loss in program state is studied under different erase conditions and correlated to cell degradation caused by HHI.

INTRODUCTION
SONOS Flash EEPROMs are gaining prominence as they are scalable, easy to fabricate and integrate with CMOS process, provide low power operation, and multi-bit per cell capability (based on localized charge storage) [1-3]. The preferred program and erase mechanisms for multi-bit operation are CHEI and BTBT induced HHI, respectively. However, two main concerns related to this P/E scheme are endurance and long-term charge retention [4-9]. The former is believed to be due to gradual build-up of electrons in ONO stack, owing to mismatch in spatial positions of injected electrons and holes. Adapted program/erase (P/E) sequence, intermediate FN anneal or FN reset can overcome this, but require large erase times or bias [5-7]. Moreover, it is debated whether retention problem is caused by lateral charge migration in ONO, or vertical charge loss [4-9]. In this work erase bias is optimized to achieve fast, single-cycle erase, which also minimizes endurance problem. Then its effect on post-cycling retention is studied, to identify the main cause behind retention problem. It is shown that charge loss is the main cause of decreased retention in programmed state, after cycling.

RESULTS AND DISCUSSION
All measurements were performed on isolated stack-gate SONOS memory cells with ONO dimensions of 5.8/8/6 nm and gate length of 0.25 µm (unless mentioned otherwise). Erase bias was varied but program bias was fixed at 8/5/0 V (bias is always specified as \( V_G/V_D/V_D \)), with source grounded. Threshold voltage (\( V_{TH} \)) is defined using constant current definition (\( I_C = 0.8 \mu A \) at \( V_D = 0.1 \ V \)).

Fig. 1 illustrates the endurance problem in a SONOS cell under CHEI/HHI operation (program and erase times, \( T_P \) and \( T_E \), were fixed during cycling). Erase state \( V_{TH} (V_{TE}) \) gradually increases with P/E cycling, and cannot be easily reduced as seen from the post-cycling transients. \( V_{TE} \) degradation is lower when fewer electrons are injected (or more holes are injected–not shown), indicating a gradual build-up of electrons in ONO (beyond the reach of holes).

The cell degradation due to P/E cycling can be studied from \( I_{CP} \) (IV), Gate Induced Drain Leakage (GIDL), and Charge Pumping (CP) characteristics as shown in Figs 2-4. Cycling degrades the slopes in linear (LS) and sub-threshold (SS) regions of IV (in programmed cell). LS is related to charges trapped near gate-drain overlap, and SS to charges trapped above channel [10,11]. The slope of GIDL curve (both programmed and erased states) degrades with cycling, indicating damage or charge build-up near gate-drain overlap region. Increase of \( I_{CP} \) with cycling, starting with the very first erase pulse, indicates interface trap (NIT) generation with HHI.

Use of slightly aggressive erase conditions reduces cycling induced window closure as illustrated in Fig. 5. Though aggressive bias improves endurance, it also increases cell degradation. The effects of erase \( V_{ERASE} \), \( V_D \), \( V_G \) and \( T_E \) on P/E cycling are summarized in Table 1. Cycling induced cell degradation plays an important role behind post-cycling data retention. This was studied at four different bias conditions; three with minimal \( V_{TH} \) degradation after 10k cycles (Fig. 6), and one with a high \( V_{TH} \) degradation. After cycling, all cells were programmed to identical \( V_{TH} \) before measuring retention loss.

Fig. 7 compares retention loss of virgin cell, to those cycled (10k) under two different erase conditions: one resulting in significant charge build-up (bad-endurance), and other with minimal charge build-up (good endurance). Better post-cycling retention following bad endurance shows that higher charge build-up need not result in higher retention loss. However, a single erase (after 10k cycles) at higher bias on the cell with bad endurance leads to a sudden increase in retention loss (\( I_{CP} \) also increases). These show a possible dependence of retention loss on NIT generation. Fig. 8 shows the IV characteristics during retention for virgin and 10k-cycled cells. SS, which is sensitive to lateral spread of trapped charge in CHE programmed cells [10,11], does not change too much during retention, indicating absence of significant lateral charge migration in these cells.

Fig. 9 compares retention at the three different bias conditions resulting in least \( V_{TH} \) degradation. Similar post-cycling retention, except for a slight improvement at lower \( V_D \), means they equally degrade the cell. Fig. 10 compares retention in virgin, single-erased, and 10k-erased cells. Even one erase degrades retention significantly, and this retention loss increases with further P/E cycling (consistent with increase in \( I_{CP} \)). In addition, retention does not show a dependence on the time elapsed between cycling and retention measurement. This too suggests that NIT degradation that does not anneal with time may be responsible for retention \( V_{TH} \) drop.

The sudden increase of retention loss in single erased cells is studied further using two different erase cases shown in Fig. 11. The first cell is erased by HHI followed by an FN reset [6], which reduces hole trapping in ONO but does not affect NIT. In the other cell HHI is done at the end, leaving trapped holes along with NIT (as verified by \( I_{CP} \)). Similar retention in both cells shows that NIT, and not hole trapping, is responsible for degraded retention after erase.

CONCLUSIONS
SONOS cells cycled using HHI erase and CHEI program show a gradual increase in \( V_{TH} \) and NIT. An aggressive erase bias can give good endurance with very fast erase times but with higher cell degradation. Greater correlation of program state retention with NIT degradation, rather than with charge build-up in ONO, suggests charge-loss to be the main cause behind retention \( V_{TH} \) drop. Trade-off between endurance and retention determines choice of erase bias.

REFERENCES
VTE increases with cycling and is worse at higher Tp. Post-cycling P/E transients show that the cell cannot be erased to initial VTE.

Figure 1. Endurance characteristics and P/E transients of a SONOS cell. VTE increases with cycling and is worse at higher Tp. Post-cycling P/E transients show that the cell cannot be erased to initial VTE.

Figure 2. Pre- and post-cycling (case A) IV characteristics show a degradation of linear and sub-threshold slopes (probe overlap and channel regions, respectively [10]) in program state.

Figure 3. Pre- and post-cycling (case A) GIDL curve (related to overlap degradation) with cycling.

Figure 4. Pre- and post-cycling (case A) CP characteristics show an increase in NIT with cycling. A large increase is seen after the very first erase pulse.

Figure 5. Effect of erase Vg and Vb on cell endurance. △VTE during cycling can be reduced by using higher |Vg| and/or |Vb|.

Figure 6. Endurance at three different bias conditions that gave minimum |△Vg| at the end of 10k cycles (Table 1). Average of 2 different runs is shown here.

Figure 7. Retention characteristics of a virgin cell and cells cycled (10k) under case A and case B (of Figs. 1 and 6). Case A shows better retention in spite of charge build-up, but it worsens with a single erase at a higher bias (case B).

Figure 8. Pre- and post-retention (5000 s) IVs for a virgin and a cycled (10k) cell. SS and LS do not change significantly during retention period.

Figure 9. Retention characteristics of cells cycled under different conditions shown in Fig. 6.

Figure 10. Retention characteristics at various stages of a cell cycled under case B (Fig. 6).

Figure 11. ICP and retention of cells erased in 2 different ways: (a) HHI followed by FN reset (NIT present without trapped holes), and (b) HHI after FN reset (both NIT and trapped holes present).

Table 1. The effects of varying erase Vb, Vg, Vb and TE. △VTH is the shift in 10k cycles. ICP is post-cycled (10k) value at Vtop = 4.4 V.