Reliability of Ultrathin JVD Silicon Nitride MNSFETs Under High Field Stressing

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Abstract—In this paper, we study the reliability of n-channel Metal-Semiconductor-Fieldeffect transistors (MNSFETs) fabricated using ultrathin Jet Vapor Deposited (JVD) Silicon Nitride gate dielectric under constant voltage stressing. Due to the stress, shifts in threshold voltage and transconductance as well as interface state generation are observed. Our study shows that degradation is polarity dependent. MNSFETs show lower degradation when the applied stress voltage is positive. We have also compared the performance of MNSFETs with conventional MOSFETs under identical stress conditions. Under positive stressing, MNSFETs clearly outperform the MOSFETs but under negative stressing MNSFETs show more degradation.

I. INTRODUCTION

Alternate high-K gate dielectrics are needed to replace conventional SiO2 in MOS transistors. Some of the alternative gate materials that have been investigated are silicon nitride, and tantalum, hafnium and zirconium oxides. However, the degradation and reliability of high-K dielectrics need to be explored in depth. Jet Vapor Deposited (JVD) Si3N4 has shown promise as an alternate dielectric with improved hot carrier performance as compared to conventional MOSFETs [1]. It has been shown to be resistant to boron penetration [2]. Conventional MOSFETs with ultrathin SiO2 gate dielectric have shown increased interface state generation under high-field stressing causing gm and Vth shifts. In MOSFETs, the degradation and hence the charge-to-breakdown QBD is known to be polarity dependent [3]-[7]. In this paper, we study the polarity dependent reliability of n-channel MNSFETs and compare performance of MNSFETs with MOSFETs under equivalent stress fields.

II. DEVICES

The devices used in this study are n-channel, n+ poly-Si gate transistors fabricated using an identical CMOS process except the gate deposition process. One set of transistors has Si3N4 as the gate dielectric deposited using the JVD process[2] followed by annealing at 800°C for 25 min in N2 (referred to as MNSFETs). The second set of transistors has SiO2 grown at 800°C followed by an in-situ anneal in N2 (referred as MOSFETs). The MNSFETs have an Equivalent Oxide Thickness (EOT) of 3.1nm and the MOSFETs have a gate oxide thickness of 3.9nm. The transistors have W x L = 10 x 0.18μm2.

III. EXPERIMENT

The transistors were subjected to high-field stressing with constant voltage applied to the gate with the source, drain and substrate grounded. The stress was interrupted periodically to monitor the changes in the gate threshold voltage Vth, transconductance gm and Vgd. The values of Vth and gm were obtained from the Id-Vgd characteristics measured at a drain bias of 50 mV. The peak transconductance was calculated from the Id-Vgs characteristics measured at a gate-bias of 50 mV and a drain bias of 5V.

IV. RESULTS

A. Pre-stress characteristics of MNSFETs and MOSFETs

The pre-stress Id-Vgs, gm-Vgs and charge pumping characteristics of MNSFET and MOSFET are compared first. The pre-stress Id-Vgs and gm-Vgs characteristics of the transistors are shown in Fig. 1. Both gm and Id are normalized with C0x.

B. Post-stress performance of MNSFETs and MOSFETs

The performance of MNSFETs and conventional MOSFETs is illustrated under identical equivalent positive stress of +12 and +14MV/cm. The peak transconductance was measured from the Id-Vgs characteristics measured at a gate-bias of 50 mV and a drain bias of 5V. The performance of MNSFETs and conventional MOSFETs is illustrated under identical equivalent positive stress of +12 and +14MV/cm. The peak transconductance was measured from the Id-Vgs characteristics measured at a gate-bias of 50 mV and a drain bias of 5V.
\(\Delta g_m\) which is defined as \(|g_{max} - g_{max,0}|\) is shown in Fig. 4. It is clear that for positive fields, MNSFETs show better performance compared to MOSFET's. Next, we compare the performance of MNSFETs with MOSFETs under negative stress fields equal to -11 and -12MV/cm. The change in \(N_{it}\), \(\Delta N_{it}\) is plotted in Fig. 5. The change in \(g_m\) is shown in Fig. 6. We can see that for negative stress fields, MNSFETs do not always outperform MOSFETs.

C. Polarity dependence of post-stress MNSFETs

The stress voltage polarity dependence in MNSFET's is illustrated for effective fields of +12MV/cm and -12MV/cm respectively. The charge pumping current \(I_{cp}\) and drain current \(I_d\) is illustrated in Figs. 7, 8, 9 and 10 respectively. The charge pumping current for positive stress is lower than that for negative stress by a factor of 4. The change in threshold voltage is also lower for positive stress. The normalized increase in \(N_{it}\) defined as \((N_{it} - N_{it,0})/N_{it,0}\) and conduction current \(|g_{max} - g_{max,0}|/g_{max,0}\) and threshold voltage \((V_{th} - V_{th,0})/V_{th,0}\) are plotted as a function of stress time in Fig. 11. We can see that compared to gate positive stress, gate negative stressing produces higher \(N_{it}\), \(g_m\) and \(V_{th}\) shifts.

V. DISCUSSION

With varying stress time, \(\Delta N_{it}\) and \(\Delta g_m\) show power law \((\alpha t^n)\) dependence for both MNSFETs and MOSFETs for both positive and negative stress. For positive stress (inversion), the exponent value \(n\) for MNSFET's varies between 0.35-0.38 for \(\Delta N_{it}\) and 0.3-0.4 for \(\Delta g_m\) which are similar to the 0.35 value (0.3) observed in p-MNSFETs subjected to constant voltage FN stress under inversion [8]. Our results show that under gate positive stress (inversion), MNSFETs show lesser \(\Delta N_{it}\) degradation than MOSFETs which has \(n\) value of 0.53. We can see that both the magnitude and rate of degradation is smaller for MNSFETs for positive stress. In case of MNSFETs, values of \(n\) for \(\Delta g_m\) is about 0.3-0.4 which is same as \(\Delta N_{it}\). In case of MOSFETs, values of \(n\) are about 0.4-0.46, slightly lower than that of \(\Delta N_{it}\). Compared to MOSFETs, MNSFETs show lower magnitude and slightly lower values of \(n\). Fig 3 and Fig 4 clearly illustrates that JVD nitrides perform better than MOSFETs under positive gate voltage stress. The threshold voltage \(V_{th}\) is an important parameter in the operation of a transistor. Both interface states and bulk trapping contribute to the variation in the threshold voltage. We have separated the two contributions and plotted \(\Delta V_{th}\) and \(\Delta V_{th}^t\) in Figs. 12 and 13 respectively. \(\Delta V_{th}\) shows power law dependence for both MNSFETs as well as MOSFETs. In case of MNSFETs, \(\Delta V_{th}\) initially increases rapidly and saturates suggesting that there are bulk traps which are filled up during stressing. This behaviour rules out bulk trap...
Fig. 5. Comparison of effect of negative stress fields on \( N_t \) in conventional MOSFETs and JVD MNSFETs. \( \Delta N_t = (N_{t0} - N_{t}) \) is plotted as a function of time.

Fig. 6. Comparison of effect of negative stress fields on \( g_m \) in MOSFETs and JVD MNSFETs. \( \Delta g_m = |(g_{m0} - g_{m})| \) is plotted as a function of time.

Fig. 7. \( I_{ds} \) plotted as a function of stress time for a JVD MNSFET stressed at \( E = +12 \) MV/cm.

Fig. 8. \( I_{ds} \) plotted as a function of stress time for a JVD MNSFET stressed at \( E = -12 \) MV/cm.

generation. In case of MOSFETs, the initial bulk trap density is lower. With stress, MOSFETs show bulk trapping which increases with time, indicating that there is trap generation.

Under negative stress, the magnitude \( \Delta N_d \) is higher for MNSFETs than MOSFETs. The exponent is about (0.3) for nitrides compared to MOSFETs (0.4). The exponent value of \( \Delta g_m \) is 0.3 for both MNSFETs and MOSFETs but the magnitude is lower for nitrides. Under negative voltage stress, MOSFETs show positive charge trapping while MNSFETs show net negative trapped charges. The degradation of \( V_{th} \) is higher in MNSFETs than MOSFETs as illustrated by Fig. 14 and Fig. 15 respectively resulting in degraded performance of MNSFETs.

MOSFETs also show polarity dependent degradation as shown in Figs. 3, 4, 5 and 6. Here also we see that the damage due to negative stress is higher compared to the positive stress. Polarity dependent degradation in ultrathin MOSFETs is attributed to the defects in the gate/dielectric interface [4], presence of a structural transition layer at the substrate/dielectric interface [5], or due to the difference in the electron energy dissipated at the anode which in turn depends on the anode Fermi level [6], [7]. According to the anode Fermi-level model, damage is maximum for p-type anodes where the electron impact generates hot holes. The defect generation rate is higher when the density of holes is larger in the anode [9]. We have used the AHI model to explain the polarity dependent degradation in MNSFETs. The band diagram of MNSFET in accumulation and inversion is shown in Fig. 16. MNSFETs show lesser \( \Delta N_d \) and
Δgm degradation than MOSFETs under positive stressing. This may be due to the higher bond breaking energy of Si-N bonds. However, under negative stress ΔNf and ΔVth shifts are higher than oxides which may be due to the increased hot-hole flux due to the smaller hole barrier height in nitrides (1.9eV as compared to 4.9eV). If an electron arrives with an energy of 3eV, impact ionizes to create a hole with a maximum energy of 3-1.1=1.9eV comparable to the SiN/Si barrier of 1.9eV. Compared to this, hole flux in SiO2/Si would be smaller where barrier height for holes is 4.9eV.

VI. CONCLUSION

MNSFETs perform better compared to the MOSFET's under positive bias which is important for n-channel devices. The nitrides show smaller Nf generation compared to the oxides under identical fields. The transconductance degradation is lower compared to MOSFETs. Also there is no bulk trap generation in MNSFETs and hence threshold voltage shifts are also smaller. We can therefore conclude that the JVD MNSFETs can easily outperform MOSFETs under gate positive condition, that is when the transistor is in inversion. However the degradation of Vth in MNSFETs is larger compared to MOSFETs under negative stress fields, that is when the surface is in accumulation although transconductance degradation is lower. By controlling the initial bulk trap density, JVD MNSFETs can be expected to outperform MOSFETs.

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Fig. 13. Effect of positive stress fields on $V_{th}$ in conventional MOSFETs and JVD MNSFETs plotted as a function of time.

Fig. 14. Effect of negative stress fields on $\Delta V_{th}$ in conventional MOSFETs and JVD MNSFETs plotted as a function of time.

Fig. 15. Effect of negative stress fields on $\Delta V_{th}$ in conventional MOSFETs and JVD MNSFETs plotted as a function of time.

Fig. 16. Band diagram of a NMOS-MNS transistor under a) Accumulation and b) Inversion.

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