A Comprehensive Trapped Charge Profiling Technique for SONOS Flash EEPROMs

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Abstract

Trapped charge profiles under CHE program of SONOS flash cells are uniquely determined and verified using I-V, GIDL and CP measurements and Monte Carlo simulations. The prospect of profiling using I-V measurement alone is discussed. The inaccuracy associated with conventional CP technique is discussed. The correct method of CP simulation for programmed SONOS devices is shown and programming induced interface-trap generation is accurately determined to predict overlap of electron/hole profiles during program/erase, length of program-gate for split-gate cells, and minimum possible gate length for 2-bit storage capability. SONOS cells use Channel Hot Electron (CHE) injection for programming and Band-Band-Tunneling (BBT) hot hole injection for erase. An important parameter is the lateral trapped charge profile, which must be determined accurately to predict overlap of electron/hole profiles during program/erase, length of program-gate for split-gate cells, and minimum possible gate length for 2-bit storage. So far, attempts were made to profile trapped charges during programming by using either subthreshold I-V (SIV) together with Gate Induced Drain Leakage (GIDL) and/or by only Charge Pumping (CP). However, reported values for trapped-charge spread show large discrepancy that must be resolved. This work uses linear I-V (LIV) with GIDL and SIV with CP to accurately determine trapped charges in gate/drain overlap and channel respectively (near the drain junction and overlap region). The prospect of using only I-V and the limitation of using only CP for profiling is shown. Obtained trapped charge distribution is verified using Monte Carlo simulations.

Experimental and simulation details

Experiments were performed on SONOS devices having top-oxide/nitride/bottom-oxide (ONO) dimensions of 5.8/8/6 nm and 0.25 μm channel length. The cell was programmed in small steps with intermediate I-V and GIDL measurements. Reverse read was used for I-V measurements at V_D=0.1V [2]. GIDL measurements were done at V_D=2V and substrate current was measured while varying V_G. CP was done at the start and the end of programming using a fixed base (-4.6V) and varying top (-4 to +4.6V) pulse having f=400 kHz. Process and device simulations were done using ISE TCAD tools. The output of device simulation was then used for Monte Carlo simulations using SMC [9].

1-I-V and GIDL

A. Effects of charges on GIDL and I-V stack

Fig. 1 shows initial I_D-V_G curves for few identical SONOS cells. Observed variation in "turn-on" behavior, subthreshold slope (SS) and threshold voltage (V_T) indicates the presence of processing induced trapped charges in ONO stack. It was reported that localized charges near source/drain edges affect the "turn-on" behavior of such cells [6]. Indeed, non-uniform trapped charges (maximum near the gate edges, decreasing gradually towards the center of channel) have been used in device simulations to match the I_D-V_G of these cells.

Fig. 2 simulates the effect of overlap and channel charges on I_D-V_G curves. Charges are placed on rectangular packets from the gate edge. Note that channel charge degrades V_T and SS while overlap charge affects GIDL [6]. However, overlap charge also modulates the carrier density in the gate/drain overlap region and increases series resistance. This degrades the linear slope of I_D-V_G curves, but does not affect SS significantly. Similar to GIDL [6], slope of linear I-V can also provide independent estimate of overlap charges. Hence, only I-V (LIV and SIV) measurements can be used to obtain full estimate of trapped charge distribution.

B. Charge profiling

Fig. 3 and Fig. 4 respectively show measured I-V (LIV, SIV) and GIDL during programming together with simulated results. Charges are placed symmetrically on both source and drain sides (in rectangular packets) to simulate the initial I-V (matching is not possible without these charges). Simulation parameters are adjusted only once to match the initial I-V with experiment. To match the I-Vs for subsequent program levels, charges are added (never removed) at the drain side. Initial GIDL curve is simulated using the charge from initial I-V and adjusting the GIDL parameters to obtain a good match. Subsequent GIDL curves are matched by adding suitable charges on the drain side. Excellent match is obtained between measurement and simulation.

Fig. 5 shows trapped charge profiles obtained from I-V and GIDL simulations and channel hot electron profile obtained from Monte Carlo simulations. Charge distribution obtained using I-V compares very well with that obtained from GIDL. Therefore, it is indeed possible to determine trapped charge distribution by using I_D-V_G measurements alone. Moreover, channel hot electron distribution supports the experimentally determined lateral spread of trapped charge distribution. The obtained spread (40nm) is similar to that reported in [6] but is ~2X smaller than in [7].
C. Sensitivity analysis

Fig. 6 shows the sensitivity of obtained charge profile. A 10% change in charge magnitude affects $V_T$ and linear-slope while a 10% increase or decrease in charge spread makes a noticeable change in $SS$. Due to such strong sensitivity, the trapped charge distribution obtained from such a method is believed to be close to reality.

Charge Pumping

A. Limitations of traditional method

In CP, the gate is repetitively pulsed from inversion to accumulation and DC current ($I_{CP}$) due to interfacial electron hole recombination is measured as shown in Fig. 7 [10, 11]. For any pulse top ($V_{TOP}$) and base ($V_{BASE}$) level, CP occurs in the portion of channel where $V_{BASE} < V_{FB} (x)$ and $V_{TOP} > V_T (x)$. $V_T (x)$ and $V_{FB} (x)$ are the local threshold and flatband voltages, and must vary monotonically from the center of the channel towards gate edge so that CP measurements (fixed-$V_{TOP}$, varying-$V_{BASE}$ and fixed-$V_{BASE}$, varying-$V_{TOP}$) can be used to profile interface traps (NIT) and trapped charges (NOT) accessible by CP. As only one measurement is usable, both $V_{TOP}$ and $V_{FB}$ must vary.

$V_{TOP}$ and $V_{FB}$ are the local threshold and flatband (x). $VT (x)$, $V_{FB} (x)$ are the local threshold and flatband voltages. Hence, CP can be seen that equal spread of the Nor and NIT are required to obtain a good match with experimental $I_{CP}$. Fig. 11 (LHS) shows experimental and simulated $I_{CP}$. It can be seen that equal spread of the $N_{OT}$ and $N_{IT}$ are required to obtain a good match with experimental $I_{CP}$. Fig. 11 (RHS) shows simulated $I_{CP}$ where $N_{IT}$ spread (inside channel) is different from $N_{OT}$ spread. Larger $N_{IT}$ spread overestimates $I_{CP}$ while a smaller spread underestimates it.

It is indeed possible to find many combinations of $N_{OT} (x)$ and $N_{IT} (x)$ that can match CP characteristics. Fig. 12 shows the experimental and simulated $I_{CP}$ for such a case. Such $N_{IT}$ however would not match $I_{CP}$ and resulting $N_{IT}$ may also be unphysical. Therefore, $N_{OT} (x)$ that satisfies all of the $I-V$, GIDL and CP data is the most likely solution.

Conclusions

$I-V$, GIDL, CP measurements and full band Monte Carlo simulation are used to uniquely determine the trapped charge profile after CHEF program of SONOS flash cells. It is shown that such profiling is also possible by measuring $I-V$ only. It is also shown that conventional CP techniques cannot be used for profiling and will lead to uncertain results. The correct method for CP simulation is shown and program induced $N_{IT}$ generation is estimated. The sensitivity of $I-V$ and CP data to obtained trapped charge profile is also analyzed.

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References

Figure 1. $I_d$-$V_G$ characteristics of various identical un-programmed SONOS cells measured on different parts of a wafer. Variations in $V_r$, SS and shape suggest presence of (processing induced) non-uniform charges in the ONO stack.

Figure 2. Simulated $I_d$-$V_G$ with different amount of charge placed in rectangular packets. Increasing channel charge spread (curve B) affects SS and $V_r$. Increasing overlap charge magnitude (curve C) degrades linear slope and $V_T$ but doesn't affect SS.

Figure 3. Measured and simulated $I_d$-$V_G$ during programming. Simulations are done by placing charges in rectangular packets (12nm in overlap, 3 packets of 10nm in channel). Initial curve is matched by placing identical charges on both source and drain sides. Programmed curves are matched by adding charges on the drain side only. A sudden decrease in linear slope at the start of program indicates large charge injection into the overlap region.

Figure 4. Measured and simulated GIDL currents during programming. Simulation parameters are adjusted by matching the initial current by using initial charge distribution obtained from I-V. Programmed curves are matched by independently (of I-V) adding charges in the drain side. Large change in $I_{GIDL}$ at the start of program also indicates large charge injection into overlap region.

Figure 5. Charge profile (drain side) obtained from I-V (Fig. 3) and GIDL (Fig. 4) simulations. Channel hot electron density obtained from Monte Carlo simulation (at programming bias) is also shown. End of ONO stack (gate edge) is at 122nm.

Figure 6. Sensitivity analysis. Changing charge spread (decreased by removing a charge packet and increased by adding a new packet) changes SS, which cannot be re-adjusted by modifying magnitude of existing charge. Increasing charge magnitude changes $V_T$ and affects slope of linear I-V.

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Figure 7. Schematic CP setup and $V_T(x)$, $V_{FB}(x)$ distribution along the channel for conventional FET. $V_{TOP}$ and $V_{BASE}$ are the top and base levels of applied pulse. Measurements are done by either fixing $V_{TOP}$ and varying $V_{BASE}$ (to track $V_{FB}(x)$) or by fixing $V_{BASE}$ and varying $V_{TOP}$ (to track $V_T(x)$).

Figure 8. Simulated $V_{FB}$ and $V_T$ profiles along the channel of initial and programmed cells (plotted in the drain side, origin corresponds to center of channel). Zero charge profiles are obtained from device simulation. Interfacial carrier concentration of $10^{10}$ cm$^{-3}$ is used to define $V_{TOP}$ and $V_{BASE}$. Initial and programmed profiles are calculated by using charges extracted from $I$-$V$ simulation.

Figure 9. (LHS) Measured $I_{CP}$ as a function of $V_{TOP}$ and (RHS) schematic of $V_T$ profile along the channel (to illustrate CP area as $V_{TOP}$ is varied, see text), for initial and programmed device. $X_0$ indicates start of CP region, corresponding to $V_T$ value $V_0$.

Figure 10. $V_T$ profile of region 'CE' and 'CDG' (Fig.9) before and after program. Initial profile is estimated from CP data. Programmed profile is obtained using the charge distribution from $I$-$V$ method (box profile is linearized by joining the mid-points that extend up to 63 nm). CP zone extends up to 110 nm (initial) and 79 nm (after program) for $V_{TOP}$=4.6V.

Figure 11. Experimental and simulated CP characteristics. Inset shows linearized $N_{OT}$ and $N_T$ profiles used for simulation. (LHS) Best fit with $\Delta N_T=0$ at 63 nm and 8.2x10$^{11}$ cm$^{-2}$ at 79 nm. (RHS) Simulations with $N_T$ spread (inside channel) 5 nm more (A) or less (B) than $N_{OT}$ spread (note that CP zone extends only up to 79 nm after program). Calculated curves over or under estimate CP current.

Figure 12. CP characteristics simulated assuming an arbitrary triangular $N_T$ distribution (whose peak corresponds to overlap charge obtained from $I_{CP}$-$V_C$). Obtained $\Delta N_T$ distribution is also shown. Such $N_T$ profile (converted back to box profile) cannot match experimental $I_{CP}$-$V_C$ characteristics.