Multi-Level Programming of NOR Flash EEPROMs by CHISEL Mechanism

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Introduction
Multi-level (ML) storage is becoming an important option to achieve high-density flash EEPROMs [1]. This is done by storing different amount of charges in the floating gate (FG) to reliably distinguish different levels and treating these levels as different combination of bits. Since large amount of charges need to be stored in FG for ML operation, faster programming is required so that the overall writing speed is not compromised. In addition, this needs to be done without much increase in programming power. Recently, Channel Initiated Secondary Electron (CHISEL) injection was shown as an excellent low power and fast programming scheme for NOR flash EEPROMs [2,3]. The performance, scalability and reliability of CHISEL were demonstrated for ML-level programming [3,4]. However, to the best of our knowledge, very few studies have focused on the feasibility of using CHISEL mechanism for ML programming [5].

This paper demonstrates the performance and reliability of flash cells under ML CHISEL programming operation. Program transients show excellent self-convergence leading to $V_T$ control. Six different bitcell doping schemes were studied and optimized doping is identified based on their program and drain-disturb performance. Cycling endurance was studied on the optimized bitcell. Programmed $V_T$ levels show very little degradation, program transients retain their self-convergence, program/disturb margin remains within limit while only the erased $V_T$ level shows some degradation after 100K cycling. The impact of bitcell scaling on the performance and reliability of ML CHISEL programming is also explored.

Results and Discussion
Experiments were performed on isolated, fully scaled ($W=0.3\mu m$) bitcells made using 0.18um technology, having floating gate length ($L_{FG}$) of 0.20-2.6um, tunnel oxide and IPD thickness of 12nm and 20nm respectively. The floating gate to control gate coupling is 0.55 and the cell area is about 0.45$m^2$. Table 1 lists the channel doping, junction depth, natural $V_T$ and junction breakdown voltage ($V_{BD}$) of different types of bitcells used in this study. Programming was done at a substrate bias ($V_S$) of $-2V$ with different control gate ($V_{CG}$) and drain ($V_D$) bias. Uniform channel erase was always done with $V_{CG}=-20V$. $V_T$ is defined as $V_{CO}$ required for 5mA drain current ($I_D$) at $V_D=0.8V$.

Figure 1 shows the ML programming transients of a $L_{FG}=0.26\mu m$ D3 bitcell at $V_{PP}=3.7V$. $V_{CO}$ was suitably adjusted to get four distinct $V_T$ levels (2, 3.5, 5 and 6.5V) with 1.5V margin. It is clearly seen that CHISEL operation offers self-convergent programming leading to excellent $V_T$ control, i.e. irrespective of starting $V_T$, programming always saturates to a $V_T$ level determined by $V_{CO}$ alone. For array operation, this unique feature will clearly help to obtain multiple $V_T$ levels with minimum use of program verification steps.

Drain disturb originates from band-to-band tunneling (BBT) and is a serious reliability concern for CHISEL operation [6]. Figure 2 shows the drain-disturb transients measured at all the four levels corresponding to Fig. 1. It is clearly seen that 00 level suffers from charge gain while 11 level is prone to charge loss. The intermediate levels are less prone to drain disturb.

Figure 3a shows $T_P$ as a function of $V_{PP}$ for different $L_{FG}=0.26\mu m$ bitcells mentioned in Table 1. For all the cells $T_P$ decreases exponentially as $V_{PP}$ is increased. Figures 3b and 3c correlate disturb time $T_D$ (time for a $V_T$ change of 0.1V) versus $T_P$ in the charge gain (00 level) and loss (11 level) disturb modes respectively for different $L_{FG}=0.26\mu m$ bitcells. $T_P$ was decreased by increasing $V_{PP}$. It can be clearly seen that CHISEL programming performance improves ($T_P$ reduces) for bitcells having higher channel doping and shallower S/D junction [7]. However this also increases BBT and drain disturb [6]. Based on the trade-off between $T_P$ and $T_D$ (at $L_{FG}=0.26\mu m$), we chose device D3 for further measurements.

Figure 4 shows the degradation of programmed and erased $V_T$ for repetitive program/erase (P/E) operation between 00 and 11 and 01 levels. Negligible degradation is observed for programmed $V_T$. This is attributed to the presence of highly populated Electron Energy Distribution (EED) tail during CHISEL programming [4,8]. Erased $V_T$ shows some degradation, which is more for P/E operation between 00 and 11 levels compared to that between 00 and 01 levels.

Figure 5 shows ML programming transients of a $L_{FG}=0.26\mu m$ D3 bitcell at $V_{PP}=3.9V$ taken before and after 100K P/E cycles (between 00 and 11 levels). Little degradation is observed in $T_P$ and in the self-converging nature of the programming transients.

Figure 6 shows drain-disturb transients corresponding to Fig. 5 measured at 00 and 11 levels before and after cycling. Charge gain disturb increases while charge loss disturb decreases. Effect of P/E cycling on drain disturb is explained by the increase in trap-assisted tunneling and reduction in BBT (because of increase in FG potential because of degradation in gate coupling coefficient) [6].

The scalability of CHISEL based ML programming was explored by studying D5 $L_{FG}=0.2\mu m$ cells. Figure 7 shows the cycling induced degradation of program and erase $V_T$ for cycling between 00 and 01 and 00 and 11 level. As before, degradation is only seen for erase $V_T$ with very small degradation in the overall $V_T$ window.

Figure 8 shows ML programming transients of a D5 $L_{FG}=0.2\mu m$ bitcell at $V_{PP}=3.9V$ taken before and after 100K P/E cycles (between 00 and 11 levels). In this case the programming was done between the two extreme levels. Once again, little degradation is observed in $T_P$ and in the self-converging nature of the programming transients, which shows the scalability of reliable ML CHISEL programming.

Conclusion
To summarize, ML programming and its associated reliability are studied in NOR flash EEPROM cells under CHISEL programming operation. Program transients show excellent self-convergence and offer good $V_T$ control. Six different types of bitcells having different channel doping and S/D junction depth were studied. Bitcell showing optimized program and drain disturb performance was identified and chosen for cycling. Cycling induced degradation was only seen for the erased $V_T$ and not for any of the programmed $V_T$ levels. Program transients retain their self-convergence and program/disturb margin remains within limit after cycling. Studies were also performed to demonstrate the scalability of reliable ML programming. Our results clearly show that CHISEL injection mechanism is well suited to handle ML programming.

References
Table 1: Doping schemes of bitcells used in this study. $V_T$ ($V_{DD}=5.5$V) and $V_{BE}$ ($V_B$ for $I_F=10$A, $V_{DD}=0$) measured on identical FG - CG shorted FETs.

<table>
<thead>
<tr>
<th>Type</th>
<th>Channel Doping</th>
<th>Junction Depth</th>
<th>Natural $V_T$</th>
<th>Junction $V_{BE}$</th>
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<tr>
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<td>Low</td>
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<td>High</td>
<td>2.21</td>
<td>7.3</td>
</tr>
<tr>
<td>D4</td>
<td>Medium</td>
<td>Low</td>
<td>2.43</td>
<td>7.0</td>
</tr>
<tr>
<td>D5</td>
<td>High</td>
<td></td>
<td>2.49</td>
<td>7.2</td>
</tr>
<tr>
<td>D6</td>
<td>High/Halo</td>
<td>High</td>
<td>2.55</td>
<td>6.8</td>
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</table>

Fig. 1: Self-converging ML programming transients (1.5V level spacing) of a $L_{FG}=0.26\mu$m cell under CHISEL operation.

Fig. 2: Drain disturb transients taken at different $V_T$ levels on a $L_{FG}=0.26\mu$m cell. Largest disturb seen for 00 and 11 levels.

Fig. 3: (a) Programming time for bitcells D1-D6 as a function of drain bias. $T_p$ was calculated for programming from 00 level to 11 level. (b) Charge gain (from 00 level) and (c) Charge loss (from 11 level) disturb time as a function of programming time (as drain bias is varied) for bitcells D1-D6. Data labels are shown in Fig. 3(b). Technologies that increase CHISEL programming efficiency also increase drain disturb. D3 cells show fast $T_p$ together with good (>10%) program/disturb margin in both charge gain and loss modes.

Fig. 4: Cycling induced degradation in program and erase $V_T$ for D3 $L_{FG}=0.26\mu$m cells under programming from 00 to 11 and from 00 to 01 levels. Degradation is seen for erase $V_T$ only.

Fig. 5: ML programming transients measured before/after 100K program/erase cycles (00 to 11 level) on a D3 $L_{FG}=0.26\mu$m cell. Degradation in the self-converging nature of the programming transients is negligible.

Fig. 6: Charge gain (from 00 level) and charge loss (from 11 level) disturb transients measured before/after 100K program/erase cycles on a D3 $L_{FG}=0.26\mu$m cell. CG increases and CL decreases after cycling.

Fig. 7: Cycling induced degradation in program and erase $V_T$ for D5 $L_{FG}=0.26\mu$m cells under programming from 00 to 11 and from 00 to 01 levels. Degradation is seen for erase $V_T$ only.

Fig. 8: ML programming transients measured before/after 100K program/erase cycles (00 to 11 level) on a D5 $L_{FG}=0.26\mu$m cell. Degradation in the self-converging nature of the programming transients is negligible.