Thin Film Single Halo (SH) SOI nMOSFETs –
Hot Carrier Reliability for Mixed Mode Applications

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Abstract—In this paper, for the first time, we report a study on the hot carrier reliability performance of Single Halo (SH) thin film Silicon-on-Insulators (SOI) nMOSFETs for mixed signal applications. The single halo structure has a high pocket impurity concentration near the source, end of the channel and a low impurity concentration in the rest of the channel. Besides having excellent dc output characteristics, better $V_{th} - L$ roll-off control, lower DIBL, higher breakdown voltages and kink free operation, these devices show higher ac transconductance, higher output resistance and better dynamic intrinsic gain ($g_m R_o$). The experimental results show that SH SOI MOSFETs exhibit a lower hot carrier degradation in small-signal transconductance and dynamic output resistance, in comparison with the conventional (CON) homogeneously doped SOI MOSFETs. From 2-D device simulations, the lower hot carrier degradation mechanism in SH-SOI MOSFETs are analyzed and compared with the conventional SOI MOSFETs.

1. INTRODUCTION

The advantages of SOI MOSFETs over their bulk counterparts are: simple dielectric isolation, elimination of latch up, reduced Short Channel Effects (SCE), better radiation performance, and lower Hot Carrier Effects (HCE) [1]. The SOI technology has also shown great potential for mixed mode and analog applications [2]. SOI also offers potential for low voltage, low power, and high-speed applications. One of the main advantages in SOI structure is that, it introduces dramatic improvement in noise decoupling between digital and analog circuits on the same substrate, because of buried oxide. The analog SOI CMOS switch has shown distinct advantages in comparison to bulk. However, the reliability performance of SOI MOSFETs is crucial for their use in deep submicron technology, particularly in System-on-Chip (SoC) applications. Till recently, reliability implications of MOSFETs in analog domain have not been reported much, because of the long channel transistors being used. However, the reduction of the effective gate length leads to a substantial increase of hot carrier effects [3].

The hot-camer induced degradation in SOI devices is more complex than that of bulk devices due to the presence of two interfaces. The aggressive scaling of devices further aggravates this problem because of an increase in the electric fields. The high electric field can provide sufficient energy to the channel carriers so as to cause impact ionization. The large number of highly energetic carriers will damage not only the front interface, but also the back interface. In fully depleted devices the carrier transport at one channel will be affected by the defect generation at the other interface.

There exists a difference between analog and digital operation concerning the device parameters of importance and their related circuit parameters. In digital operations, circuit delay is the dominant circuit parameter; therefore drain current drive capability is the most important device parameter to be considered as a measure of degradation. No doubt this is an important parameter in analog case too, but we have to also consider device parameters like threshold voltage and small-signal parameters, like transconductance and drain conductance, which have direct implications on the performance of an analog circuit. In an analog circuit good matching is an essential demand, as paired or exactly weighed devices are used, whose properties will determine the accuracy of differential stages and current mirrors. The most common degradation is the threshold voltage shift by the charges trapped at the opposite oxide interface because of interface coupling effects [4]. Degradation in the threshold voltage and drain current will increase the mismatch between analog-paired devices. This will adversely affect the offsets, accuracy, and resolution of the circuit. The other CHC induced degradations occur in gain, frequency response, and linearity, due to the degradation of small-signal parameters of the device. The degradation in the noise will increase the signal to noise ratio of the circuit.

Typically, CMOS device design has been optimized for digital applications even for aggressively scaled channel...
length devices. However the same rules may produce a poor analog performance due to short channel effects (SCE). Thus it becomes necessary to optimize the existing CMOS logic technologies, so that they are compatible with the conventional CMOS process, and at the same time lead to improved performance in mixed-mode systems. MOSFET device design has been engineered by different approaches for the alleviation of these disadvantages. Different approaches like source/drain engineering, channel engineering and gate work function engineering have been implemented for the alleviation of these disadvantages. Channel engineering has been widely used to improve the short channel performance. Asymmetric single halo (SH) MOSFET structures have been introduced for bulk [5-6] as well as for SOI MOSFETs [7] to adjust the threshold voltage and improve the device SCE and hot carrier effects (HCE). These devices also achieve higher drive current by exploiting the velocity overshoot phenomenon [5], which is an advantage in mixed mode analog/digital circuits.

Reliability studies have previously been performed on channel-engineered bulk devices under digital operation [8-9] and it has been found that SH bulk devices outperform the conventional homogeneously doped devices. The reliability implications of SH bulk p-MOSFETs under analog operating conditions have also been reported [10]. It is therefore necessary to evaluate the analog reliability implications of CON and SH SOI nMOSFETs. In this paper we have shown that SH SOI nMOSFETs have superior hot carrier reliability performance in comparison to CON devices. The other advantages of SH over CON SOI MOSFETs, like absence of kink, lower inherent parasitic bipolar junction transistor (pBJT) gain have also been reported elsewhere in detail [11-12]. The small-signal characteristics for mixed mode applications of deep submicron, thin film SH SOI MOSFETs have been reported recently [13].

To evaluate the hot-carrier reliability performance of MOS devices in analog operation, a different approach has to be followed compared to the evaluation in digital domain, because the operating points of MOS transistors in digital and analog CMOS circuits differ significantly. The different degradation mechanisms which affect the device under analog operating conditions are channel hot carrier (CHC) stress, bias temperature (BT) stress and oxide stress [14]. Among these CHC stress and BT stress need specific analog approaches. This is necessary so as to reveal the relevant information for analog operation. The CHC stress can occur while the device is in the active mode, while the BT and oxide stress can occur while the device is in the power down mode [14].

2. DEVICE FABRICATION

The devices used in this work are fabricated on SIMOX wafers. Standard CMOS technology has been used for the fabrication. The CON SOI and SH SOI n-MOSFETs have been fabricated on the same wafer. The threshold voltage adjustment of the CON-SOI MOSFETs is done before the gate oxidation, whereas the implant for the SH SOI devices is done after the gate formation at a tilt angle of 15° from the source side. E-beam lithography is used to define the polysilicon gate. The thickness of the gate oxide, Si film and buried oxide are approximately 3.9 nm, 50 nm, and 180 nm respectively. The devices had a source/drain extension in addition to deep source/drain junction. A two-step Titanium silicidation process with Ge pre-amorphization is implemented to control the silicide depth and reduce the series contact resistance. The first step anneal is 450°C, 3 min followed by a selective etch to remove TiN and unreacted Ti. The second step is 780°C, 30 s.

3. EXPERIMENTAL RESULTS AND DISCUSSIONS

To study the CHC stress under analog operations, the device parameters of importance are transconductance, output conductance, gate voltage shift (offset voltage), and drain current. Due to the absence of body contact in SOI MOSFETs it is not easy to find the bias points (VDS, VGS) at which the maximum CHC damage will take place i.e. where normally the maximum substrate current occurs. A bias point was chosen, assuming that the worst case for CHC degradation is approximately at VDS = VDD/2 [15]. The devices were stressed up to 10,000 s to find the time dependence of the degraded parameters. The crucial analog parameters, transconductance, output resistance, and offset voltage were measured under small-signal analog operating conditions using different methodologies. However post-stress measurement conditions were kept identical to the pre-stress measurements. AC small-signal measurements were made using HP 4284 LCR meter at a frequency of 10 kHz with signal level of 10 mV.

Experiments were performed to see the degradation of different parameters as a function of stress time. The devices were stressed under DC stress conditions at VDS=4 V and at VGS= VDD/2 V. The drain current shift ΔID_d/d obtained in a single device will appear as a current shift in an analog circuit [16]. Fig. 1 shows the shift in the saturation drain current measured at fixed VDS= VDD of 0.2 V for both CON and SH SOI nMOSFETs. Under identical stress conditions it is observed that SH SOI MOSFET shows lesser degradation. Fig. 2 shows the degradation in the gate voltage for CON and SH devices. The post-stress gate voltage was measured at VDS=0.7 V to get a drain current value (0.1 mA) under typical analog operating conditions. The post-stress gate voltage was measured such that the same VGS=0.7 V produced the same value of pre-stress current. It is again seen that less degradation occurs in SH device in comparison to its CON counterpart. The degradation
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mechanism in deep submicron SOI MOSFETs has been explained [17] assuming a stress-induced trapping of electrons near the drain. The length of the zone containing occupied electron traps and/or charged interface states is a function of stress time. The degradation in the analog operation has been described [14] for bulk MOSFETs and has been attributed to the stress-induced shift of the pinch off point of stress time. This behavior in transconductance has been observed for different silicon film thicknesses and channel tilt implants, though the percentage shift is different. The marginal decrease in transconductance degradation for SH after about 2000 s can be attributed to the reduction in the threshold voltage. The reason may be the electrons, which are injected towards the gate oxide, act as a drain extension thereby reducing the effective gate length. The lower reduction in transconductance degradation can be attributed to the much lower lateral electric fields in the SH SOI MOSFET. It has also been explained [8] as due to the peak impact ionization of asymmetrical (here SH) device being located further away from the surface of the device than in the conventional nMOS device [18]. The Fig. 4 shows degradation in the output drain conductance for CON and SH devices. The drain conductance degrades faster in CON than in SH devices.

Fig. 1: Time evolution in saturation drain current degradation under DC stress conditions. Drain current was measured at $V_{DSS}=0.7$ V and $V_{GS}=V_{th}+0.2$ V.

Fig. 2: Time evolution in gate voltage degradation under DC stress conditions. Gate voltage was measured, to produce the same pre-stress current at $V_{DSS}=0.7$ V. The measurement was done at small-signal for $V_{GS}=10$ mV and $f=10$ kHz.

Fig. 3: Time evolution in transconductance degradation under DC stress conditions. Transconductance was measured at $V_{DSS}=0.7$ V and $V_{GS}=V_{th}$ to produce the same pre-stress current. The measurement was done at small-signal for $V_{GS}=10$ mV and $f=10$ kHz.

Fig. 4: Time evolution in output conductance degradation under DC stress conditions. Output resistance was measured at $V_{DSS}=0.7$ V and $V_{GS}=V_{th}+0.2$ V.
Virgin SH SO1 MOSFETs were also stressed in the reverse mode i.e. halo doping on the drain side, achieved by reversing the source and drain. The DC stressing conditions were kept same. It was observed that degradation in transconductance and drain current was large even compared to CON SO1 MOSFETs. The large degradation in reverse mode is attributed to the higher peak of electric field near the drain junction, which results due to the halo being near the drain side. To understand this, simulated electric fields were plotted for the various cases. The actual process parameters used in the fabrication were fed to the process simulator Tsuprem4 [19]. The device generated from Tsuprem4 was used as an input to the device simulator Medici [20]. The simulated lateral electric field from the device simulator Medici, near the drain junction, under typical DC stressing condition of \( V_{DS} = 4 \) V and \( V_{GS} = V_{DS}/2 \) for CON, SH forward mode, and SH reverse mode are shown in Fig. 5. The illustration clearly shows the peak electric field is highest for SH reverse mode of operation, whereas SH forward mode has lower peak of lateral electric field than the CON SO1 MOSFET. Thus SH in forward mode will have better reliability than the CON SO1 MOSFETs.

![Simulated lateral electric field profiles](image)

**Fig. 5:** Simulated lateral electric field profiles (near the drain junction), along the channel at \( V_{DS} = 4 \) V for CON, SH forward mode and SH reverse mode at 4 nm below the interface.

### 4. Conclusion

In this paper we have investigated the hot carrier reliability concerns of deep submicron SH SO1 nMOSFET in comparison to CON SO1 MOSFETs. The analog operating conditions and related stresses have been considered. We have shown from experimental characterization that thin film single halo SO1 MOSFETs are very effective in the suppression of various hot carrier degradation compared to CON devices under identical stress conditions. The reasons for lower degradation are looked into from 2-D device simulations. Thus SH SO1 MOSFETs are excellent candidates for analog and mixed mode applications.

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### References


