Device Degradation of n-channel Poly-Si TFTs due to High-Field, Hot-Carrier and Radiation Stressing

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1. Introduction
For many years polysilicon has been used in planar silicon integrated circuit technology for gates and interconnects. Over the last few years, there has been increasing interest in polysilicon Thin Film Transistors (TFTs) for many high-performance applications, particularly in high-resolution displays. For these applications the primary requirement is that the TFTs should have a low threshold voltage, low and stable leakage current and reasonably high mobility [1-4]. The poly-Si TFTs typically have sufficiently large mobilities to be used for high-drive and moderately high-frequency applications. However, since low temperatures are used in the fabrication of poly-Si TFTs, both semiconducting and insulating layers are of poorer quality than those used in crystalline-Si technology. Consequently, long term stability of the TFT is an important issue. A considerable amount of research has focused on the stability of poly-Si TFTs. The instabilities are basically associated with hot carrier injection and degradation, negative gate bias instability and gate-induced carrier injection and trapping [5]. This leads to degradation of several device parameters such as threshold voltage, mobility, transconductance, and subthreshold slope. The work presented here is a comprehensive study of degradation in low temperature (≤600 °C) poly-Si TFTs due to high-field, hot-carrier and ionizing radiation stressing. This unified approach makes it possible to identify the key reasons for degradation. Furthermore, a systematic study of the dependence on device geometry, as reported here, also helps us to understand the degradation mechanisms.

2. Device Fabrication
The experimental TFTs were fabricated on polysilicon using a simple low-temperature process (≤600 °C). Silicon wafers with 500 nm thermally grown oxide were used as starting substrates. A 100 nm silicon layer was deposited at 550 °C in amorphous form by LPCVD. The amorphous silicon was then recrystallized for 20 hours in nitrogen ambient at 600 °C. After silicon island definition, 100 nm thick gate oxide was deposited by APCVD at 400°C. This was followed by the deposition of a 250 nm thick poly gate layer by LPCVD. Source, drain and gate electrodes were doped by self-aligned phosphorus implantation. The dopants were activated during densification of the low temperature oxide (LTO) at 600 °C for 10 hours in oxygen ambient. After this active device fabrication, the device was passivated by deposition of oxide by APCVD to protect it from external influences. Then contact windows were opened followed by aluminum deposition and patterning of the contact pads. Finally, the devices were hydrogenated using H2 RF plasma for 2 hours. It is worth pointing out that the hydrogenation used was not optimized. Fig. 1 shows the cross-section of the TFT device.

3. Experiments and Results
Detailed electrical characterization was performed on n-channel TFTs with channel length (L) in the range 3–30 μm and channel width (W) in the range 6–200 μm with the bulk of the device floating and source grounded. To estimate the appropriate stressing voltage for the TFT devices, experiments were first performed to find the breakdown gate voltage, which was around 30-40V. Our stressing experiments were performed by applying a high gate voltage and small drain voltage for high-field oxide stressing, high gate and drain voltages for hot carrier stressing, and exposure to γ-rays for radiation stressing. During high-field stressing, we monitored the gate current. At pre-selected time intervals, the stressing was interrupted and I-V transfer characteristics were measured. These experiments are described in detail in the sections that follow. Device

Figure 1: Cross-section of the thin film transistor (TFT).
parameters like threshold voltage, subthreshold slope, and mobility were extracted from \( I_d-V_{GS} \) (transfer) characteristics. All measurements were performed at room temperature.

4. Degradation Under High-Field Stressing

To determine the stability and lifetime of poly-Si TFTs, high-field stressing is one of the tests which is commonly done. We have done constant-voltage high-field stressing by applying large gate voltages. Characterization of the TFT devices was done before and after stressing. During stressing, the gate bias \( V_{GS} \) was kept below 30 V at all times to avoid breakdown of gate oxide and \( V_{DS} \) was maintained at 0.1 V to avoid hot carrier effects. The constant-voltage high-field stressing experiments have been performed on TFTs with different \( W \) and \( L \) values and for different stressing biases applied to the gate. Devices were stressed up to 10,000 seconds. Figure 2 shows the linear \( I_d-V_{GS} \) characteristics of a device with \( W/L = 6 \mu \text{m}/10 \mu \text{m} \) before and after the application of high-field stress with the Si in inversion \( \left( V_{GS} = 20 \text{V}, V_{DS} = 0.1 \text{V} \right) \) at room temperature. An approximately parallel shift towards the right in the device characteristics indicates that oxide trapped electrons in the oxide are the major reason for damage. The gate current decreases during stressing, confirming the phenomenon of trapping of the injected majority charge carriers (electrons) in the gate oxide. Table I summarizes the TFT parameters calculated from transfer characteristics before and after application of the high-field stress. These results show that there is an increase in threshold voltage and subthreshold (or pseudo-subthreshold [3]) slope with stressing, while mobility is almost constant. It can also be noticed that the total degradation is quite small, indicating that these devices will probably show good long-term reliability.

### Table I: Parameter variation due to high-field stressing at \( V_{GS} = 20 \text{V} \) for a transistor with \( W/L = 6 \mu \text{m}/10 \mu \text{m} \).

<table>
<thead>
<tr>
<th>StressTime (s)</th>
<th>( V_T ) (V)</th>
<th>( \mu ) (cm²/Vs)</th>
<th>( S ) (V/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-stress</td>
<td>7.29</td>
<td>1.27</td>
<td>1.46</td>
</tr>
<tr>
<td>10</td>
<td>7.56</td>
<td>1.27</td>
<td>1.80</td>
</tr>
<tr>
<td>100</td>
<td>7.66</td>
<td>1.27</td>
<td>1.85</td>
</tr>
<tr>
<td>1000</td>
<td>7.76</td>
<td>1.26</td>
<td>1.95</td>
</tr>
<tr>
<td>10000</td>
<td>7.89</td>
<td>1.23</td>
<td>2.05</td>
</tr>
</tbody>
</table>

These results suggest that the degradation is likely to be due to electron trapping in the gate oxide and mid-gap defect generation in bulk polysilicon or interface state generation. Electron trapping in the oxide leads to threshold voltage increase, and generation of interface states (at the Si/SiO₂ interface) and/or mid-gap states in the poly-Si, degrade the subthreshold (or pseudo-subthreshold) slope but not the mobility which is low to start with.

When the stressed samples were annealed at room temperature for 5 days, there was a shift of the \( I_d-V_{GS} \) characteristics back towards the pre-stress one. This is consistent with the detrapping of electrons from relatively shallow traps in the oxide [6,7]. It was also found that with higher \( V_{GS} \) during stressing, there is greater degradation, indicating more charge trapping. High-field stressing in accumulation \( \left( V_{GS} = -20 \text{V}, V_{DS} = 0.1 \text{V} \right) \) was done on a fresh device with \( W/L = 6 \mu \text{m}/15 \mu \text{m} \) to confirm the carrier type involved in degradation. It was found that there is no shift in transfer characteristics after stressing. However, there is, in this case too, a decrease of gate current during stressing. This shows that there is some electron injection and trapping, but because injection is now from the gate, much of the electron trapping takes place near the gate/oxide interface, which has negligible effect on the \( I_d-V_{GS} \) characteristics, since the gate oxide is quite thick (100 nm).

We also explored the effect of varying transistor \( W \) and \( L \) on the degradation due to high field stressing. Devices with varying channel widths and constant channel length as well as varying channel length and constant channel width were stressed in inversion \( \left( V_{GS} = 20 \text{V}, V_{DS} = 0.1 \text{V} \right) \) up to 10000 s. All devices showed shifts in threshold voltage \( V_T \) with stress time, but the extent of degradation was found to be dimension dependent. Table II shows the threshold voltage shift.

### Table II: Shift in threshold voltage (\( \Delta V_T \)) due to high-field stressing at \( V_{GS} = 20 \text{V} \) for 10000 s for various geometries.

<table>
<thead>
<tr>
<th>( W = )</th>
<th>( L = 20 \mu \text{m} )</th>
<th>( 10 \mu \text{m} )</th>
<th>( 5 \mu \text{m} )</th>
<th>( 3 \mu \text{m} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 ( \mu \text{m} )</td>
<td>0.59 V</td>
<td>0.59 V</td>
<td>0.41 V</td>
<td>0.40 V</td>
</tr>
<tr>
<td>20 ( \mu \text{m} )</td>
<td>0.15 V</td>
<td>—</td>
<td>0.28 V</td>
<td>—</td>
</tr>
<tr>
<td>50 ( \mu \text{m} )</td>
<td>0.09 V</td>
<td>0.11 V</td>
<td>0.13 V</td>
<td>0.10 V</td>
</tr>
</tbody>
</table>
shifts due to high-field stressing after 10000 s. From these data, we notice that the extent of degradation is almost same for devices having the same width, irrespective of channel lengths. However, decreasing W causes an increase in the degradation. The behavior of degradation being independent of channel length can be explained if we assume that the generation of defects during the high-field stressing occurs near source or drain edges, and not in the main channel region. So the degradation is independent of L. One may explain the inverse proportionality of degradation with channel width W by considering the device as a parallel combination of many narrower transistors of "standard" width, each of which has a potential weak spot or defect. So if a TFT device with channel width W has n such defects, then a device with width 2W would have 2n defects. Now if a device starts leaking (due to soft breakdown) from any one of the defects, then there will be very little chance of any other defect starting to leak. So in a large width device the fraction of degraded "standard" transistors will be less than that of small width device. Hence there will be less degradation in large W devices. However, to confirm this hypothesis, more experiments need to be designed and performed.

B. Degradation Under Hot-Carrier Stressing
Hot-carrier effects leading to long-term instabilities have long been recognized as one of the important limitations on the reduction of feature size. In short-channel MOSFETs, carriers acquire sufficient energy from the electric field near the drain and are injected into the gate oxide. This leads to trapping of carriers in the gate oxide and/or creation of interface states at the Si/SiO₂ interface which results in threshold voltage and mobility shifts.

We have performed hot-carrier-stressing experiments on TFTs with different W/L ratios and different VDS and VGS values. We took care not to exceed VDS = 15 V for hot-carrier stressing, having checked that this voltage produces almost no high-field stress degradation. The VGS value used was 15 V. Fig. 3 shows the I_D-VGS characteristics of a device (W/L = 50 µm/3 µm) before and after hot-carrier stress (VGS = 8V, VDS = 15V) for times up to 10,000 s. Another device with the same dimensions was stressed at VGS = VDS = 15 V up to 10,000 s and I_D-VGS characteristics for this are shown in Fig. 4. It can be seen that there is considerable shift in the curves with stressing time. The subthreshold curves (not shown here) also show considerable skewing. Although for crystalline-Si bulk MOSFETs, the degradation is most significant at VGS = VDS/2 stressing, here we find more degradation at VGS = VDS. This is consistent with our earlier result of substantial electron trapping occurring in the oxide. However, we do also see some mobility degradation due to interface-state and/or mid-gap [4, 7] state generation. These degradation results are summarized in Table III.

Hot carrier stressing was also performed on many devices with varying W and L for stressing voltages of VGS = 8 or VDS = 15 V and VDS = 15 V for differing times up to 10000 s.

![Figure 3: I_D-VGS (transfer) characteristics of a TFT with W/L = 50 µm/3 µm before and after hot-carrier stressing for various times with VGS = 8 V and VDS = 15 V.](image)

![Figure 4: I_D-VGS (transfer) characteristics of a TFT with W/L = 50 µm/3 µm before and after hot-carrier stressing for various times with VGS = 15 V and VDS = 15 V.](image)

**Table III:** Parameter changes due to hot carrier stressing for a transistor with W/L = 50 µm/3 µm.

<table>
<thead>
<tr>
<th>VGS (V)</th>
<th>VDS (V)</th>
<th>Stress Time (s)</th>
<th>ΔVt (V)</th>
<th>Δµ (cm²/Vs)</th>
<th>ΔS (V/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>15</td>
<td>100</td>
<td>0.05</td>
<td>-0.16</td>
<td>0.08</td>
</tr>
<tr>
<td>8</td>
<td>15</td>
<td>1000</td>
<td>0.24</td>
<td>-0.48</td>
<td>0.25</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>100</td>
<td>0.29</td>
<td>-0.14</td>
<td>0.34</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>1000</td>
<td>0.83</td>
<td>-0.47</td>
<td>0.62</td>
</tr>
</tbody>
</table>
15V and VDS = 15V. These experiments (whose data are not shown here) indicate that with increase in L, there is a decrease in degradation which is quite acceptable due to the fact that lateral electric field in the channel increases with decrease in L. There was almost no effect on degradation for varying W, as expected, but unlike what was seen for high-field stressing.

C. Ionizing (Gamma) Radiation Stressing Effects

To conclude our study of poly-Si TFT device degradation, stressing with ionizing (gamma) radiation was done at room temperature without bias (device open circuited), using a Cobalt-60 gamma ray chamber. In order to reduce the effect of edges, we initially used large dimension devices. Figure 5 shows the transfer characteristics of a device (W = L = 20 μm) before and after various doses of radiation. A positive shift in transfer (I_D-VGS) curves again indicates that electron trapping in the gate oxide is the major physical damage. This indicates that, unlike the case for bulk Si MOSFETs where hole trapping is the major degradation mode under ionizing radiation, here for the poly-Si TFTs we see mainly electron trapping. Radiation stressing was also done on devices with varying W and L. The degradation was almost independent of W, but depended on L. Figures 6 and 7 show the characteristics for devices with W = 20 μm and L = 10 μm and L = 3 μm respectively. These results show that for the smaller length device (L = 3 μm) there is mainly net hole trapping, unlike the longer device (L = 20 μm), where there is net electron trapping. Further, for medium length (L = 10 μm) devices, for the initial phase of irradiation there was net hole trapping, followed by net electron trapping. A 16 hr annealing without bias at room temperature shows, in all cases, a trend of recovery towards the pre-rad curve. This is because of detrapping of electrons and holes.

![Figure 5](image)

Figure 5: I_D-VGS (transfer) characteristics of a TFT with W/L = 20/20 μm before and after exposure to gamma radiation of various doses. Note in this case a rightward shift in the characteristics with increasing dose, indicating net electron trapping.

![Figure 6](image)

Figure 6: I_D-VGS (transfer) characteristics of a TFT with W/L = 20 μm/10 μm before and after exposure to gamma radiation of various doses. Note in this case an initial small leftward shift, followed by a rightward shift.

![Figure 7](image)

Figure 7: I_D-VGS (transfer) characteristics of a TFT with W/L = 20 μm/3 μm before and after exposure to gamma radiation of various doses. The device was floating during irradiation. Note in this case a leftward shift in the characteristics with increasing dose (except the highest dose), indicating net hole trapping.

4. Discussion

Although some of the results obtained by us can be explained using crystalline-Si MOS theory, other results are quite different. These new degradation effects can be attributed to the fact that in poly-Si TFTs, the deposited silicon has many grain boundaries, the deposited gate oxide has many defects and traps (especially electron traps), and also the Si/SiO₂ interface is expected to be of poorer quality in comparison to that of grown oxide on crystalline-Si MOS devices.
There are a number of factors which can cause device degradation under electrical stress: (1) gate oxide electron or hole trapping (2) generation of mid-gap defects in the poly-Si bulk and (3) generation of traps at the Si/SiO₂ interface [6]. From all our stressing results it is evident that the dominant mechanism of degradation in poly-Si TFTs is gate oxide electron trapping, which can be seen (to a greater or lesser extent) in all the different stressing modes. Under high-field stressing, decreasing gate current with increasing stressing time, parallel rightwards shift in transfer characteristics, and detrapping of carriers during the anneal phase all lead us to conclude that electron trapping in gate oxide is the major cause of degradation. Stressing in the accumulation region also shows electron trapping. Degradation in subthreshold slope with high-field stressing are probably not due to electron trapping (which should only result in parallel shifts). Rather, this may be due to generation of some mid-gap defects in the bulk poly-Si near the equilibrium Fermi level, since it is known that subthreshold (or, more correctly, pseudo-threshold [4]) currents in TFTs are dominated by such defects.

For hot-carrier stressing, we again see $V_T$ shifts which indicate oxide electron trapping [8]. However, in this case, generation of interface states at the Si/SiO₂ interface also contributes to the damage. Our results also show that there is more degradation under hot carrier stressing with $V_{DS} = V_{DS} = 15V$ than with $V_{DS} = 8V$, $V_{DS} = 15V$. This result is in contrast to mono-crystalline silicon devices where maximum degradation is usually seen for stressing bias $V_{DS} = V_{DS}/2$. This is again in part due to the large electron trapping in the gate oxide which the condition $V_{DS} = V_{DS}$ favors. Finally, the results of gamma-ray radiation stressing also show that gate oxide is very prone to electron trapping. Unlike high-field and hot-carrier stressing, where the origin of degradation is injection of (mainly) electrons from the channel or gate into the gate oxide, the mechanism at play during irradiation is generation of hole-electron pairs (HEPs) in the oxide due to radiation. So, here one would expect to see both hole and electron trapping, with hole trapping dominating, because of the much larger capture cross-sections for hole traps compared to electron traps in SiO₂. This is indeed what is observed in mono-Si MOS devices with thermally grown oxide. In our case, we did see net hole trapping for small channel length devices. This may be due to some edge effect, which we do not fully understand yet. For medium length devices, initially we see net hole trapping, and then, or higher doses of radiation, it is electron trapping, which starts dominating the degradation mechanism. This indicates that there is a high density of electron traps in the deposited oxide, which slowly start get filled (because of their smaller capture rates) and eventually dominate over the trapped holes. For longer devices, we see only net electron trapping.

From these discussions, we conclude that electron trapping in the gate oxide is the major contributor to the degradation in performance of poly-Si TFTs. The low-temperature deposited oxides necessary for these devices have a large concentration of electron traps. Other mechanisms which are involved to a lesser extent are generation of mid-gap defects in the bulk poly-silicon and generation of interface states at the Si/SiO₂ interface.

5. Conclusion

Degradation in low-temperature poly-Si TFT devices has been studied for high-field stressing, hot-carrier stressing as well as gamma radiation stressing. The degradation is dominated by electron trapping in the gate oxide that causes a parallel rightward shift in the transfer ($I_D-V_{DS}$) curves. The other probable mechanisms which are involved (though to a much lesser extent) are generation of mid-gap defects in the bulk polysilicon and creation of interface states at the Si/SiO₂ interface. The results obtained can be explained to be due to the low-temperature oxide deposition technique (APCVD) used, which results in a SiO₂ with a large number of as-grown electron traps.

References