100 nm Channel Length MNSFETs using a Jet Vapor Deposited Ultra-thin Silicon Nitride Gate Dielectric

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Abstract
Metal-Nitride-Semiconductor (MNS) FETs having channel lengths down to 100 nm with a novel Jet Vapor Deposited (JVD) SiN insulator as gate dielectric are fabricated and characterized for their electrical performance. By employing the charge pumping technique, the interface quality of SiN and its effect on the transistor performance are evaluated. We show that, compared to conventional SiO2 MOSFETs, the SiN devices show lower gate leakage current, competitive drain current drive and transconductance, good interface quality, and reduced hot-carrier degradation.

Introduction
Jet Vapor Deposited (JVD) SiN has been shown to exhibit excellent electrical properties as a MOS gate dielectric [1]. Compared to thermal SiO2, it is well known that JVD nitrides show more than an order of magnitude lower leakage current in the direct tunnelling regime for identical gate capacitance. Its excellent resistance to boron penetration and easy integration into conventional CMOS process make it a viable alternative to conventional SiO2 for scaled CMOS [2]. However, issues concerning the lower Si-SiN energy barrier and the quality of nitride-silicon interface require further study especially in the sub-100 nm channel length MOSFET regime. In this work, we present experimental results on conventional SiO2 MOSFETs and MNSFETs with channel lengths down to 100 nm. Using detailed charge-pumping studies, we probe the nitride-silicon interface properties in 100 nm channel MNSFETs and compare their performance with conventional SiO2 MOSFETs.

Device Fabrication
Two sets of N-FET’s were fabricated in the same device run in exactly the identical fashion except for the gate insulator. E-beam lithography was used to define channel lengths down to 0.1 μm [3]. One set of devices were made of SiN gate dielectric deposited at room temperature using the JVD process, followed by post deposition annealing at 800 °C for 25 min in nitrogen. Another set of devices were made by growing the gate oxide at 800 °C in dry oxygen, followed by an in-situ nitrogen anneal. A two-step Ti silicidation process with Ge preamorphization was performed to control the silicide depth and to reduce series resistance [4].

Results and Discussion
Fig. 1 shows the split-CV characteristics for a conventional SiO2 MOSFET and a JVD MNSFET. The estimated equivalent oxide thicknesses (EOT) from inversion capacitance are 3.9 nm for SiO2 and 3.1 nm for JVD nitride. Fig. 2 shows the gate leakage current in inversion for JVD nitrides and control oxides for various film thicknesses [2]. The JVD nitrides show more than an order of magnitude lower gate leakage which is mainly due to its higher physical oxide thickness (nearly twice as thick as SiO2 for equal gate capacitance) since the relative dielectric constant is estimated to be about 6.5 for JVD nitrides [2]. Fig. 3 shows the output characteristics, normalized to gate EOT, for 100 nm channel length conventional and JVD transistors. It can be seen that the JVD nitrides show identical drain current drive as compared to SiO2 MOSFETs.

Fig. 4 shows the charge pumping current (Ipump) as a function of pulse top-top level (Vtop) for a SiO2 MOSFET and JVD MNSFET. The maximum Ipump as a function of channel length is plotted for the estimation of average interface-state density (Nsi) for JVD nitride and SiO2 in 100 nm channel length MOSFETs. As can be seen, the Nsi for the JVD nitride is higher than the SiO2 by a factor of 2. Fig. 5 shows the normalized transconductance (gms) as a function of Vg for a L=100 nm JVD and conventional MOSFET. Although the gms at low gate biases is lower for JVD device, it crosses over the SiO2 MOSFET for higher Vg values. Fig. 6 shows the saturation transconductance (gmsat) (at Vto=Vds=1.5V) and sub-threshold slope (S) as a function of L for the JVD and SiO2 MOSFETs. The measured gmsat is consistently higher for JVD MNSFETs, and the less than 5% degradation in sub-threshold slope in JVD MNSFETs compared to SiO2 MOSFETs is essentially due to the slightly higher Nsi in JVD nitride as shown in Fig. 4(b).

Figs. 7 and 8 show the stress induced incremental charge pumping current (ΔIpump) as a function of Vtop and the generated interface-state density (ΔNsi) profile along the channel for a L=100 nm conventional and JVD MNSFET. Stressing was performed at identical peak substrate current (Ip) condition for realistic comparison. It is evident that ΔIpump and hence ΔNsi generation is lower in JVD MNSFETs. Figs. 9 through 11 show maximum ΔIp, and % Ip degradation (normalized to Ip) as a function of stress time, supply voltage and channel length. JVD nitride clearly shows a lower degradation indicating improved robustness against hot-carrier stressing in spite of the lower energy barrier (2.1 eV) compared to the conventional oxides.

Conclusion
MNSFETs with channel lengths down to 100 nm are fabricated with ultra thin JVD SiN as gate dielectric. Compared to the conventional SiO2 MOSFETs, JVD MNSFETs show lower gate leakage current, competitive interface quality, transconductance, drain current drive, and improved robustness. These results clearly show that JVD nitride is an excellent candidate for replacing SiO2 in the direct tunneling regime.

References
[3] B. Cheng et al., ESSDERC-98, Bordeaux, France
Fig. 1. Split-CV characteristics for Conv. and JVD MNSFET. Estimated EOT values from inversion capacitance are shown.

Fig. 2. Measured gate leakage currents for Conv. and JVD gate oxides.

Fig. 3. Output characteristics for 0.1 μm channel length Conv. and JVD MNSFET.

Fig. 4. (a) Pre-stress charge pumping current as a function of pulse top level for 0.1 μm MOSFET (b) Maximum charge pumping current is plotted as a function of channel length for extraction of average N_{it} as shown.

Fig. 5. Transconductance (at V_D=50 mV) for 0.1 μm channel length Conv. and JVD MNSFET.

Fig. 6. Saturation transconductance and sub-threshold slope as a function of channel length for Conv. and JVD MNSFET.

Fig. 7. Post-stress charge pumping current as a function of pulse top-level for Conv. and JVD MNSFET.

Fig. 8. Post-stress interface state density distribution along the channel for 0.1 μm channel length Conv. and JVD MNSFET.

Fig. 9. Normalized charge pumping current and % γ_{ns} degradation as a function of stress time for 0.1 μm channel length Conv. and JVD MNSFET.

Fig. 10. Normalized charge pumping current and % γ_{ns} degradation as a function of stress V_D for Conv. and JVD MNSFET.

Fig. 11. Normalized charge pumping current and % γ_{ns} degradation as a function of channel length for Conv. and JVD MNSFET.