Computationally Efficient Methodology for Analysis of Faulted Power Systems With Series-Compensated Transmission Lines: A Phase Coordinate Approach

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Abstract—A capacitor in series with a transmission line is protected from overvoltage due to a large fault current by a nonlinear metal–oxide varistor (MOV) connected in parallel. Fault analysis, as well as the evaluation of performance of the transmission protection system, in the presence of MOV action becomes complex because 1) v-i characteristics of the MOV are nonlinear; 2) unsymmetrical MOV action for unsymmetrical faults will introduce coupling in sequence networks; and 3) MOV action will influence voltage or current inversion phenomenon. This paper presents a computationally efficient and simple methodology for fault analysis wherein the linear part of the network is modeled by an equivalent multipoit Thevenin network. The proposed approach handles nonlinearity in fault analysis efficiently. It also provides an elegant approach to model unbalance in a network due to MOV action. The proposed approach can be used to determine relays prone to voltage or current inversion. Results on a real-life 716-bus Indian system illustrate the efficiency of the proposed approach.

Index Terms—Current inversion, fault analysis, metal–oxide varistor (MOV), series capacitor, Thevenin equivalent circuit, voltage inversion.

I. INTRODUCTION

THE capacitive series compensation of transmission lines is primarily used to enhance the power transfer capability of the existing transmission corridor. It is an attractive solution, given the limitations of the right of way and large cost of new transmission lines. Currently, many long transmission system corridors in India at 400 and 220 kV are being augmented using series compensation schemes. However, series-compensated transmission lines increase the complexity of:

1) fault analysis;
2) distance protection.

In this paper, we first focus on the problem of fault analysis with series-compensated transmission lines. Subsequently, we use this analysis to evaluate the performance of a transmission protection system.

When a series compensation scheme is deployed, the series capacitors then have to be protected against overvoltage due to the passage of fault current through them. This is usually achieved by a metal–oxide varistor (MOV) which is connected in parallel to the capacitor. However, MOV action introduces the following complexities in the fault analysis problem.

1) v-i characteristics of an MOV are nonlinear. The impedance offered by the MOV can be estimated if the value of fault current is available. However, the magnitude of fault current will depend upon the impedance offered by MOV. This interdependence can only be resolved by an iterative process, which leads to the iterative nature of the fault analysis program.
2) In case of unsymmetrical faults, such as the single-line-to-ground (SLG) fault at the capacitor terminals, MOV in all three phases may not conduct. For example, for an SLG fault on the “a” phase, MOV on the “b” phase may conduct. This introduces unbalance in the network. In turn, it implies that in the fault analysis, the advantage of decoupling in sequence networks cannot be exploited anymore. Thus, in the fault analysis program, the coupling of sequence networks has to be modelled.

When the embedded network itself is unbalanced (e.g., distribution system, action of MOVs), the attractiveness of sequence-network-based fault analysis is lost. In such a scenario, modelling directly in the phase domain is advocated [1]–[6]. Consequently, the admittance matrix grows by a factor of three. However, due to the large and sparse nature of the admittance matrix, there is practically no noteworthy loss in computational efficiency in solving the system of (1) in phase domain

\[
[Y_{bus}^{abc}]_{3n \times 3m} [V^{abc}]_{3m \times 1} = [I^{abc}]_{3n \times 1} \tag{1}
\]

instead of solving the three decoupled system of (2) in the sequence domain

\[
[Y_{bus}^{i}]_{n \times n} [V^{i}]_{n \times 1} = [I^{i}]_{n \times 1}, \quad i \in \{0,1,2\}. \tag{2}
\]

Analysis in three-phase domain is also attractive because modelling complex faults is comparatively straightforward [4]. In contrast, modeling of the series and simultaneous fault in the sequence domain requires intricate sequence domain interconnections.

Surprisingly, not much work has been reported on fault analysis with systems having MOV and series capacitors. Coursol et al. [7] and Mahserejian et al. [8] deal with the iterative approach to fault analysis for systems having series-compensated lines in sequence domain. Gopalakrishnan et al. [9] have addressed this problem in three-phase domain wherein, at each iteration of short-circuit analysis, the following sparse three-phase system of equations has to be solved:

\[
[Y_{bus} + Y_{fault}(n)]V_{phase}(n + 1) = I_{phase}. \tag{3}
\]
The fault matrix $Y_{\text{Fault}}(h)$ is updated at each iteration. While this approach is straightforward, it does not provide computational efficiency as the coefficient matrix in (3) has to be refactorized at each iteration.

Therefore, in this paper, using the phase-domain analysis, we propose a methodology to model the MOV-protected series compensator without the need for admittance matrix refactorization. We develop a multiport three-phase block Thevenin circuit model for the power system with the following noteworthy features.

1) The linear part of the system is represented by a minimal Thevenin equivalent circuit.
2) The nonlinear part of the system (i.e., MOV and series compensation) along with the fault is modelled as a load on this Thevenin equivalent circuit.
3) As a consequence of the circuit decomposition into an equivalent linear network and a nonlinear load, nonlinear albeit iterative analysis is restricted to terminal nodes of the Thevenin network. This implies that:
   • we can now achieve simplicity in modelling and analysis of nonlinear apparatus, faults, or abnormalities in short-circuit analysis;
   • modification is required to an existing short-circuit analysis program to model nonlinearity and/or unbalances in apparatus or fault is minimal and, hence, it can be achieved with ease;
   • computational effort is required to compute short-circuit currents and is practically reduced to that of a simple traditional short-circuit analysis run.

This paper is organized as follows. Section II develops the methodology of fault analysis with series-compensated transmission lines. In Section III, the fault analysis algorithm is presented. Section IV summarizes the model for the series capacitor and MOV combination [10]. Section V discusses the results of fault analysis on a 716-bus system. Section VI investigates the influence of a series compensation scheme on the performance of a transmission protection system. Section VII concludes this paper.

II. PROPOSED METHODOLOGY

The development of the mathematical model for fault analysis with series compensation involves the following steps.

Step 1) computation of Thevenin equivalent impedances;
Step 2) computation of Thevenin voltages;
Step 3) modelling of fault and MOV-protected series capacitor branch.

A. Computation of Thevenin Equivalent Impedances

In the proposed approach, the linear and balanced power system subnetwork is modelled by a multiport Thevenin equivalent circuit (see Fig. 1). For the sake of illustration, we have considered an SLG fault at bus “k” in Fig. 1. Bus “k” in general, need not correspond to either bus “i” or “j.” Typically, the boundary nodes correspond to the capacitor nodes and the node(s) having fault(s). A nonlinear and unbalanced subnetwork consisting of a series compensator along with MOV and fault impedance is seen as a load by the Thevenin equivalent.

Remark 1: To compute Thevenin equivalent impedance, we must disconnect the capacitors from the network. The Thevenin equivalent impedance can be computed by solving the following linear system of equations:

$$[Y_{\text{abc}}] \cdot [V_{\text{abc}}] = [e_{k}^i] \cdot ke\{a,b,c\}$$

where, for example, $e_{k}^i$ represents the unit current injection at “k”-phase of node-“i.” Note that $Y_{\text{abc}}$ has to be factorized only once and the block, forward and backward substitution, has to be invoked nine times. All computations are performed using block matrices with each element of coefficient matrix being a $3 \times 3$ block and the right-hand side as a $3 \times 1$ vector. For details on the design of a sparse linear system solver, reADERS are referred to [11].

B. Computation of Thevenin Voltages

There are two possible approaches for the computation of Thevenin voltage sources.

1) Approach I: A direct approach to the computation of Thevenin voltages would be to run a prefault load flow study with the series capacitor disconnected. The bus voltages at the capacitor nodes and faulted node(s) will correspond to Thevenin voltages in Fig. 1. Note that load-flow analysis gives positive-sequence voltages which can be converted to three-phase values.

2) Approach II: In this approach, we conduct prefault load-flow analysis with series compensation in the system. Consequently, we obtain the terminal voltages $V_i$, $V_j$, and $V_k$ and capacitor currents as shown in Fig. 1. From these values, we have to work back Thevenin voltages.

Remark 2: Fault impedance $Z_F$ is not considered during load-flow analysis in either of the approaches I or II.

3) Comparison of Approach I and II: With hindsight, we can say that approach II is more accurate than approach I. The reason lies in the nonlinear nature of load-flow equations. If the
system model in load-flow analysis was linear (e.g., imagine a dc load flow), then capacitor current (see Fig. 1) obtained from approach I or II would be identical. However, due to the nonlinear nature of load-flow analysis, these two values do not match. Since the final condition corresponds to the connection of the series capacitor in the network, it is better to model it in the load-flow analysis and then back to calculate the Thevenin voltages. Hence, approach-II is used in this work.

**Algorithm**
The algorithm for simulating the response of MOV in three-phase coordinates is as follows.

1) Compute the Thevenin equivalent voltages and impedances (see Fig. 1). Set iteration count $n = 1$. Neglect the MOV action and compute fault and capacitor currents.

The governing equations are

$$
\begin{bmatrix}
V_{th}^i \\
V_{th}^j \\
V_{th}^k
\end{bmatrix}
- 
\begin{bmatrix}
Z_{ii} & Z_{ij} & Z_{ik} \\
Z_{ji} & Z_{jj} & Z_{jk} \\
Z_{ki} & Z_{kj} & Z_{kk}
\end{bmatrix}
\begin{bmatrix}
I_i \\
I_j \\
I_k
\end{bmatrix}
= 
\begin{bmatrix}
V_i \\
V_j \\
V_k
\end{bmatrix}
$$

(5)

$$
\begin{bmatrix}
I_i \\
I_j \\
I_k
\end{bmatrix}
= 
\begin{bmatrix}
Y_F & \left[ V_i \right] \\
Y_F & \left[ V_j \right] \\
Y_F & \left[ V_k \right]
\end{bmatrix},
$$

(6)

Note that all elements such as $Z_{ii}, Z_{ij},$ etc. are $3 \times 3$ block matrices in phase domain and voltages and currents, such as $V_i$ and $I_i$ are $3 \times 1$ vectors in the phase domain. Substituting (6) in (5), we obtain a reduced $9 \times 9$ system of equations as follows:

$$
\begin{bmatrix}
I + Z_{TH}Y_F
\end{bmatrix}
\begin{bmatrix}
V_i \\
V_j \\
V_k
\end{bmatrix}
= 
\begin{bmatrix}
V_{th}^i \\
V_{th}^j \\
V_{th}^k
\end{bmatrix}.
$$

(7)

From (7), we work out terminal voltages and from (6), we compute capacitor and fault currents.

2) If the analysis shows that MOV will not conduct, then the existing results are adequate and we exit the fault analysis module, else go to the next step.

3) Compute MOV impedance $Z_{mov} = f(V_{mov})$, where $V_{mov}$ is the voltage across the MOV and function $f$ models the nonlinear behavior of the MOV. Also, compute $Z_{eq}$, which is the equivalent impedance of the parallel combination of the series capacitor and MOV. Compute $I_{mov}(n)$. 

4) Update the fault model $[Y_F]$ based on the latest estimates of MOV impedance. Update the capacitor terminal voltages using (7) and calculate the currents flowing through the MOV $I_{mov}(n + 1)$ and series capacitor $I_{cap}(n + 1)$.

5) Check the mismatch between $I_{mov}(n + 1)$ and $I_{mov}(n)$. If the mismatch, in an absolute sense, is less than a predefined tolerance, then it indicates convergence to the solution. Otherwise, increment $n$ by one, and proceed to 3) for the next iteration.

**III. MOV MODELLING IN FAULT ANALYSIS**

In the literature, MOV models for Electromagnetic Transient Program (EMTP) analysis [12] as well as static short-circuit analysis [10] are discussed. Goldsworthy [10] has proposed a model where in net impedance of the series capacitor and MOV combination (refer to Fig. 2) is expressed as a function of line current $I_{line}$

$$Z_{eq}(I_{pu}) = R'_C(I_{pu}) = jX'_C(I_{pu})$$

for $I_{pu} > 0.98$

(8)

where

$$R'_C = X_C\left(\frac{0.0745 + 0.49}{-35e^{-0.243I_{pu}} - 0.6e^{-1.4I_{pu}}}\right)$$

and

$$X'_C = X_C(0.1010 - 0.00574I_{pu} + 2.088e^{-0.3566I_{pu}})$$

(9)

(10)

where $I_{pu}$ is the normalized compensator current

$$I_{pu} = \frac{I_{line}}{I_{pr}}.$$ 

(11)

Typically, the capacitor protective level current $I_{pr}$ is equal to 2 to 2.5 times the rated current of the capacitor. If $I_{pu} < 0.98$, the MOV is out of the circuit and, hence, $Z_{eq} = -jX_C$. In Fig. 3, we plot the variation of normalized $R'_C$ and $X'_C$ as a function of $I_{pu}$.

From Fig. 3, it can be inferred that for low fault current, the imaginary part of the equivalent impedance for the series capacitor and MOV combination dominates the real part (i.e., capacitive effect dominates the resistive effect of the MOV). However, as the fault level increases, MOV resistance drops down significantly. Therefore, the net impedance and capacitive contribution drop down.

**Remark 3:** If Goldsworthy’s model is used for analysis, then in the proposed algorithm, steps 2 and 3 can be modified as follows.

Step 2) Compute $I_{pu}$. If $I_{pu} \leq 0.98$, then MOV will not conduct.

In such a case, existing results are adequate and we exit the fault analysis module. If $I_{pu} > 0.98$, then proceed to the next step.
Step 3) From (9) and (10), calculate the equivalent impedance for the parallel combination of series capacitor and MOV, i.e.,

\[ Z_{eq}(I_{pu}) = R_c^e(I_{pu}) - jX_c^e(I_{pu}). \]  \( \text(12) \)

From \( Z_{eq}(n) \), determine the impedance of the MOV

\[ \left( \frac{1}{Z_{NKE}(n)} \right) = \left( \frac{1}{Z_{eq}(n)} \right) - \left( \frac{1}{Z_{cap}(n)} \right). \]  \( \text(13) \)

For a nonconducting MOV, \( Z_{NKE}(n) \) is infinite.

Remark 4: If the fault is on one of the capacitor nodes, then MOV response can be simulated with either the multiport Thevenin equivalent network (Fig. 1) or two-port Thevenin equivalent network (Fig. 4).

The voltage on the faulted bus can be computed from the following equation:

\[ [I + Z_{THY_F}] \begin{bmatrix} V_i \\ V_f \end{bmatrix} = \begin{bmatrix} V_i^* \\ V_f^* \end{bmatrix}. \]  \( \text(14) \)

However, it is interesting to note that the model described by Fig. 1 and (7) is generic enough to handle the particular case of a fault on a capacitor node. The equivalence between the two circuits (Figs. 1 and 4) is established in the Appendix.

IV. RESULTS

We have carried out fault analysis on a 716-bus system which is an adaptation of the Northern Region Electricity Board (NREB) system of India. Details of the network are shown in Table I. Parameter ranges considered by Goldsworthy for the development of the linearized model and corresponding values of MOV used in this study are given in Table III.

For the purpose of this study, the power system network with the series-compensated transmission line is simulated with varying degrees of compensation ranging from 1% to 35% in steps of 1%. Throughout the study, we assume that the value of \( I_{pr} \) is fixed at 2400 A. The line current flowing through the series capacitor and MOV combination as well as the fault current are plotted against the degree of compensation. In these studies, we have simulated the fault on the “a” phase of one of the capacitor nodes (i.e., on the “j”th node) as shown in Fig. 4. The results obtained with the two-port Thevenin equivalent network model in Fig. 4 are consistent with the multiport Thevenin equivalent network model in Fig. 1. With the tolerance set to 0.00001 p.u. (on the 100-MVA base), the maximum number of iterations required to converge to the solution is 11, with 7 being the typical value.

The results obtained with the proposed method (Figs. 5 and 6) are validated with an existing method [9] (Figs. 7 and 8). Table II compares the effort required by the proposed approach
Fig. 7. Validation of the line current with a degree of compensation using the existing method [9] \(I_{\text{text}} = 144.3\) A.

Fig. 8. Validation of the fault current with a degree of compensation using the existing method [9] \(I_{\text{fault}} = 144.3\) A.

vis-a-vis approach in [9]. It shows that the method described in [9] requires an effort that is approximately equal to seven short-circuit analysis runs. In contrast, the effort required by the proposed approach is equivalent to one run of the short-circuit analysis. This is because 1) LU factorization of the large \(3n \times 3n\) admittance matrix is performed only once, 2) only two block forward and backward (F/B) substitutions are required with a large coefficient matrix \((3n \times 3n)\), and 3) the effort required for the iterative process which involves seven linear system solvers with a coefficient matrix of size 6 is negligible.

For the sake of analysis, in this study, the fault current and line current have been observed for the following two cases.

Case 1) When MOV action across the capacitor is not modelled.

Case 2) When MOV action across the capacitor is modelled.

A. Case 1: MOV Action Not Modelled

When MOV is not modelled, the line current (the current flowing through the path A-B-C marked with the dotted line in Fig. 4) increases as the degree of compensation is increased until the capacitive reactance cancels the inductive reactance component of \(Z_{\text{eq}}\). At the peak point, the line current is limited by only the resistance and mutual impedances of the Thevenin equivalent circuit. Beyond this point, as the degree of compensation increases, capacitive reactance dominates and the A-B-C path impedance increases. As a result, the line current reduces.

The correctness of the line current waveform when MOV is not modelled (Figs. 5 and 6) is validated with the traditional method of calculating fault current in phase coordinates [9] (Figs. 7 and 8).

B. Case 2: MOV Action Modelled

When MOV action is modelled, the following observations can be made from Figs. 5 and 8.

1) As the degree of compensation is increased, the fault current reduces.

2) A threshold value of compensation exists that is below the fault current (neglecting MOV action) that is more than what is obtained by modelling the MOV action and vice-versa.

3) In the limiting case of compensation tending to zero, the fault current when MOV action is modelled is lower in comparison to the case when the MOV action is not modelled.

These observations can be explained as follows.

1) Observation 1: The operating region of the MOV series capacitor combination is shown in Fig. 9. In this study, we notice that irrespective of the degree of compensation, the MOV series capacitor combination presents predominantly resistive burden, which increases with an increase in the degree of compensation. \(I_{\text{pu}}\) in this study varied from 3.18 to 4.7, and \(|Z_{\text{eq}}|\) varied from 0.0002 to 0.0105 p.u. Hence, as compensation is increased, the fault current decreases.

2) Observation 2: Fig. 10 shows the plot of net impedance from the dominant source (bus-"A") to the fault node (bus-"F"), as a function of the degree of compensation. When the MOV action is not modelled, we see that as the degree of compensation increases, net impedance reduces up to a threshold point and then increases. In contrast, with MOV modelling, net impedance increases gradually with an increase in the degree of compensation. Hence, an intersection point exists, which determines the threshold degree of compensation, below which the fault and line current neglecting the MOV action is more than when it
is considered. Beyond this threshold, the MOV and series capacitor combination presents lower impedance than the series capacitor alone (i.e., neglecting MOV). This is reflected in a reciprocal fashion in current behavior.

3) Observation 3: This can be explained by observing the difference in impedance offered with and without MOV modelling (see Fig. 10). In the limiting case, when MOV is modelled, it presents an additional finite impedance value. This reduces the fault current.

Remark 5: The proposed method is generic enough to model arbitrary faults at arbitrary locations. Further, if at a later stage, new models for MOV are proposed, it will not affect the proposed method. Also, there is no restriction on the number of faulted nodes. There can be a string of faulted nodes in the network. For every additional faulted node, the size of the MOV per (9) and (10). There can be a string of faulted nodes in the network. Further, if at a later stage, new models for MOV are proposed, it will not affect the proposed method. However, the probability of a relay malfunction during current inversion is significantly reduced by the operation of an MOV which effectively bypasses the capacitor. Thus, if one wants to evaluate the probability of, say, a backup relay, maloperation, then MOV action has to be properly addressed in the short-circuit program.

In case fault current levels are large enough to result in MOV operation, the observation on step change in impedance is not strictly true. For example, if the MOV introduces a very small resistance in parallel to the capacitor, the capacitor will be practically bypassed. Since, the distance relays base decisions on the phasor model of the faulted system, a short-circuit program, which models MOV action, can be used as an analysis and design tool.

Distance relays in the presence of series-compensated lines may maloperate due to either voltage or current inversion [14]. For a fault in the vicinity of the series capacitor, apparent impedance seen by a primary relay can be capacitive. Consequently, it may fail to operate and thereby compromise dependability. In contrast, the apparent impedance seen by a distant relay (e.g., a backup relay), looking toward the fault and carrying a significant contribution of fault current may be inductive. Further, the overreach effect, which is a consequence of the presence of the series capacitor, may cause the distance relay to maloperate. The probability of a backup(s) relay malfunctioning due to voltage inversion is significantly reduced by the operation of an MOV which effectively bypasses the capacitor. Thus, if one wants to evaluate the probability of, say, a backup relay, maloperation, then MOV action has to be properly addressed in the short-circuit program.

In case of current inversion, impedance seen by all of the relays, which feed the fault current through the capacitor, is capacitive. This endangers the dependability of the distance protection scheme. However, the probability of a relay malfunction due to current inversion is also significantly reduced by MOV operation which provides an effective bypass for the series capacitor. Thus, modelling of the MOV in a short-circuit program is required for analyzing the performance of a transmission protection system.

If at a relay location, voltage or current inversion is a likely event, then the distance relay will have to be either modified or replaced with more modern relays which overcome the direction determination problem by use of, say, memorized prefault polarizing voltages.

In the context of the 716-bus system, Table IV shows the impedance seen by a backup relay, on an adjacent line, for the SLG fault which was discussed in the previous section. It can be seen that:

1. when the degree of compensation is large, the impedance seen by the distance relay is in the IVth quadrant. Hence, the relay will not pick up.
2. when we compute impedance values, with and without MOV modelling, we notice that MOV modelling causes impedance seen by the relay to be more inductive. A similar observation has been made in [12] by using EMTP analysis.
3. Conversely, a relay looking away from the fault may incorrectly pickup.
4. This is the classical case of voltage inversion.
5. Segregated phase comparison scheme [15, p. 504] provides an effective way for primary protection of the series capacitor-protected transmission systems. It is immune to the voltage inversion problem but it may fail to pickup during current inversion. However, the chances of current inversion are usually negligible.
TABLE IV

<table>
<thead>
<tr>
<th>Degree of Compensation</th>
<th>Apparent Impedance (Without MOV)</th>
<th>Apparent Impedance (With MOV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>35</td>
<td>0.0345 - j 0.1924</td>
<td>0.2108 - j 0.0577</td>
</tr>
<tr>
<td>5</td>
<td>0.0762 - j 0.0126</td>
<td>0.088 + j 0.0113</td>
</tr>
<tr>
<td>1</td>
<td>0.0805 + j 0.0103</td>
<td>0.0828 + j 0.015</td>
</tr>
</tbody>
</table>

- when percentage compensation is small, the impedance offered by the equivalent branch \( R_e' - jX_e' \) is also small and, hence, no significant effect of MOV modelling is observed. Further, apparent impedance seen by the relay falls in the 1st quadrant.

We envisage the requirement of such studies to be more common, at least in the Indian context, as use of the series-compensated lines becomes more predominant to enhance transmission system capacity.

VI. CONCLUSION

In this paper, we have proposed a computationally efficient approach for fault analysis with series-compensated transmission lines. In this method, we decompose the network into two subnetworks. The first subnetwork is typically linear and balanced. It can be modelled by the Thevenin equivalent circuit. The nonlinear and unbalanced subnetwork, typically comprised of fault and a combination of series capacitor and MOVs is presented as a load on the Thevenin equivalent circuit. This leads to the following improvements in the analysis:

1) Computational efficiency, as \( Y_{11} \), has to be factorized only once.
2) Elegance due to direct mapping on to the Thevenin equivalent.
3) Programming ease as existing short-circuit analysis programs in three-phase coordinates can be easily modified to incorporate series capacitor and MOV models.

The presence of series capacitors in the transmission system introduces the possibility of voltage or current inversion. Determination of likely locations where voltage or current inversion may be observed, requires modelling of the MOV action as it influences impedance calculations. The proposed tool can be effectively used to analyze the performance of a transmission protection system in the presence of MOV-protected series capacitors.

APPENDIX

The equivalence between the two circuits (Figs. 1 and 4) can be seen by treating the node “k” as a dummy node which is identical to the faulted capacitor node (say “j”). Therefore, \( V_{th} = V_{th}' \) and \( Z_{kk} = Z_{jj'} \), \( Z_{ik} = Z_{ij} \), \( Z_{ki} = Z_{ji} \), \( Z_{kk} = Z_{jj} \), and \( Z_{jk} = Z_{jj} \) (i.e., we substitute “k” in place of “j”). Now we can split the \( j \)th branch of the Thevenin equivalent circuit in Fig. 4 into two branches as shown in Fig. 11.

From Fig. 11(a), we can write the fault current equation as follows:

\[
I_f = I_f + I_{jj'},
\]

To ascertain the equivalence of this approach, we also have to verify that in Fig. 11(b), \( V_{x}^2 = V_{x} = V_{f} \). To achieve this objective:

1) voltage drop \( (Z_{jj}I_{ij}) \) due to mutual coupling between \( i \)th and \( j \)th nodes should be duplicated in both branches of Fig. 11(b) (i.e., \( Z_{ii} = Z_{jj} \));
2) to account for the self-impedance base voltage drop \( Z_{jj}(I_{f} + I_{jj}) \) in Fig. 11(a), we introduce the mutual coupling of \( Z_{jj} \) between the nodes “j” and “k” in Fig. 11(b). Hence, \( Z_{kk} = Z_{kj} = Z_{jj} \).

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REFERENCES

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