Abstract—A simple and novel measurement technique to obtain three-port network-parameters of MOS transistors from two-port measurements on a single test structure is presented. The measured data is used in the form of a lookup table (LUT) for RF circuit simulation. It is shown that simulation results obtained with the LUT approach for a 2.4-GHz low-noise amplifier match very well with measurements, thus demonstrating the usefulness of the LUT approach. It is also shown that, for high frequencies, it is important to use the tables of $y$-parameters actually measured rather than those interpolated from low-frequency measurements. This is illustrated with a tuned amplifier simulation example.

Index Terms—Circuit simulation, lookup table (LUT), modeling, MOSFETs, RF CMOS, three-port measurement.

I. INTRODUCTION

WITh continuous downsizing of the CMOS technology, the cutoff frequency of the MOSFET has reached the gigahertz regime, making it suitable for RF applications [1]. Advances in CMOS technology have enabled fabrication of passive elements like on-chip inductors, MIM capacitors for which accurate models have been developed [2]. To correctly predict the circuit behavior and to reduce design cycles, it is necessary to have compact MOSFET models which are accurate in the RF frequency range.

Most of the compact models for the MOSFET are based on the quasi-static (QS) approximation. However, when the operating frequency is close to the device cutoff frequency, the QS assumption fails to accurately predict the device behavior [3]–[5]. Several models have been proposed for the MOS device in the RF range [5]–[7] to account for the non-QS (NQS) effects. These models predict the performance of the circuit with reasonable accuracy at high frequencies [8] but often require time-consuming and complicated optimization routines. Apart from NQS effects, extrinsic effects such as parasitic capacitances and inductances can no longer be ignored at high frequencies. This makes analytical modeling difficult.

The lookup table (LUT) approach has been an attractive alternative for circuit simulation [9], and efficient interpolation algorithms have been developed for implementation of the LUT approach in circuit simulators (e.g., see [10]). In the LUT approach, the exact behavior of the device is accounted for without any approximations, and thus the long and difficult compact model development phase is avoided.

For a complete LUT description of a MOS transistor, the device must be considered as a three-port device, and three-port microwave characteristics of the device must be obtained. Techniques to obtain three-port microwave characteristics from two-port measurements have been reported in the literature [11]–[16]. However, these approaches require different test structures and often involve complicated analysis. Characterization involving different test structures introduces device-level variations in the measurements. In addition, the terminating impedance interferes with the dc-biasing of the device [13], [15].

The purpose of this paper is to: 1) demonstrate extraction of three-port characteristics of the MOS transistor from two-port measurements using a simple technique and 2) demonstrate the application of the LUT approach for analysis of MOS transistor circuits at RF.

The paper is organized as follows. Section II presents a novel technique to obtain three-port $s$ - or $y$-parameters using a two-port network analyzer and only one test structure. Section III presents the LUT approach for both small- and large-signal analysis. Simulation results using the LUT model are presented and compared with measurements. Section IV presents a simulation example to demonstrate the importance of using the actual high-frequency data in the LUT approach.

II. THEORY AND MEASUREMENT

Any n-port network is fully characterized by its n-port-parameters like $s$, $y$, $z$, and $h$ which are inter-convertible. At RF, the two-port $s$-parameters are easily and accurately measured using a network analyzer. For $n > 2$, a multiport network analyzer can be used to characterize the network; however, it is not commonly available.

Techniques have been reported to obtain n-port-parameters from two-port $s$-parameters [11]–[16]. In [15], three-port $s$-parameters of a dual-gate FET were obtained by assembling two-port $s$-parameters of special test structures. These two-port $s$-parameters directly correspond to the entries of the characteristic
3×3 $s$-parameter matrix as the third port of the test structures has been terminated using the 50-Ω characteristic impedance. This procedure has some inherent drawbacks. In the RF regime, where the deembedding of shunt parasitics is needed, the use of different device structures in the measurement can give incorrect results. More importantly, the 50-Ω termination at the third port interferes with the DC biasing of the device, especially when the drain of the FET is terminated [13], [15]. This is not a problem if passive devices like power dividers and couplers are characterized.

Here, we describe a general scheme to obtain three-port-parameters from a suitable set of two-port measurements. Our approach is much simpler and more cost-effective as compared to previously published work. The method is especially attractive for active devices since it does not interfere with biasing of the devices.

### A. $y$-Parameters

For any $n$-terminal device, the $n \times n$ $y$-parameter matrix has the following property [4]:

$$\sum_{j=1}^{n} y_{jk} = \sum_{k=1}^{n} y_{jk} = 0$$  \hspace{1cm} (1)

where the subscripts correspond to the terminals of the device. The MOSFET, being a four-terminal device, has a total of 16 $y$-parameters. Because of (1), we need to find only nine of these to completely characterize the device. Defining the bulk node as the common terminal (ground), a MOSFET then has three ports: gate bulk, drain bulk, and source bulk. The nine small-signal $y$-parameters associated with these three ports of the MOSFET are defined by

$$\begin{bmatrix} i_g \\ i_d \\ i_s \end{bmatrix} = \begin{bmatrix} y_{gs} & y_{gd} & y_{gd} \\ y_{ds} & y_{dd} & y_{ds} \\ y_{bs} & y_{bd} & y_{bd} \end{bmatrix} \begin{bmatrix} v_g \\ v_d \\ v_s \end{bmatrix}$$  \hspace{1cm} (2)

where $s, d, g,$ and $b$ stand for source, drain, gate, and bulk terminals, respectively.

Let the port source bulk be ac-shorted externally with a suitably large capacitor and the signal $v_s$ set to zero. We define this as the “GD” configuration and use it to find the following two-port $y$-parameters

$$Y^{GD} = \begin{bmatrix} y_{gs} & y_{gd} \\ y_{bs} & y_{bd} \end{bmatrix}.$$  \hspace{1cm} (3)

These-parameters are obtained from two-port $s$-parameters using a two-port network analyzer. Similarly, by making $v_{db}$ and $v_{gd}$ zero, we define GS and SD configurations, respectively. Fig. 1(a) illustrates these configurations. The two-port $y$-parameters associated with the GS and SD configurations are given by

$$Y^{GS} = \begin{bmatrix} y_{gs} & y_{ge} \\ y_{se} & y_{sd} \end{bmatrix}.$$  \hspace{1cm} (4)

$$Y^{SD} = \begin{bmatrix} y_{sb} & y_{sd} \\ y_{db} & y_{dd} \end{bmatrix}.$$  \hspace{1cm} (5)

We finally obtain the $3 \times 3 y$ matrix simply by assembling the two-port $y$-parameters as shown in Fig. 1(b).

This technique requires only a single device to be measured in three two-port configurations. The external ac short is achieved by using a ground/power/ground (GPG) probe which provides about 120-pF shunt capacitance at the port terminals. Note that...
III. LOW-FREQUENCY LUT-LF

At low frequencies, the device can be assumed to be operating in the quasi-static regime, and the following equation holds for terminal currents:

$$I_x(j\omega) = \sum_{i=gd,lbs} \left( \frac{\partial L_x}{\partial V_i} + j\omega \frac{\partial Q_x}{\partial V_i} \right) V_i(j\omega)$$  \hspace{1cm} (7)

where $x$ can be gate, drain, bulk, or source. $I_x$ and $Q_x$ are functions only of the instantaneous terminal voltages, and they can be obtained directly from the measured $y$-parameters. These constitute the low-frequency LUT for the device which can be directly used for small-signal analysis. For large-signal analysis, we need $Q_x$ as a function of the terminal voltages which can be obtained by integration [19], [20] as illustrated in Section III-A. Note that, since the measured data is available only at discrete values of bias voltages, suitable interpolation schemes need to be employed for circuit simulation. We have used the interpolation scheme described in [10] and implemented the LUT model in the public-domain circuit simulator SEQUEL [21].

A. Terminal Charge Extraction

Although the focus of this work is on small-signal analysis, it is instructive to observe that the terminal charges required for large-signal analysis can be obtained simply by integration of the measured $y$-parameters. The imaginary part of the $y$-parameters gives the capacitance: $\omega C_{xy} = Im(y_{xy})$. Since $C_{xy} = \partial Q_x/\partial V_y$, we can compute the terminal charges by integrating the $y$-parameters along suitable integration paths. For example, the gate charge ($Q_G$) can be obtained by integration along the following equivalent paths:

$$\omega Q_G(V_{GS}, V_{DS}, V_{DS}) = \int_{0}^{V_{DS}} \text{Im}(y_{gd}(0, V_{DS}, 0)) dV_{ds}$$

$$+ \int_{0}^{V_{GS}} \text{Im}(y_{gs}(V_{gs}, V_{DS}, 0)) dV_{gs}$$

$$+ \int_{0}^{V_{DS}} \text{Im}(y_{gd}(V_{GS}, V_{DS}, V_{bs})) dV_{1s}$$  \hspace{1cm} (8)

$$\omega Q_G(V_{GS}, V_{DS}, V_{DS}) = \int_{0}^{V_{DS}} \text{Im}(y_{gd}(0, 0, V_{bs})) dV_{bs}$$

$$+ \int_{0}^{V_{GS}} \text{Im}(y_{gs}(0, V_{bs}, V_{DS})) dV_{gs}$$

$$+ \int_{0}^{V_{DS}} \text{Im}(y_{gs}(V_{gs}, V_{DS}, V_{DS})) dV_{gs}.  \hspace{1cm} (9)$$

Fig. 4 shows $Q_G$ obtained by numerical integration of the measured $y$-parameters along these two paths. The two results are in excellent agreement and thus provide a good additional
check on the measured results. We have also verified that the variation of the various terminal charges with respect to the bias voltages is in qualitative agreement with that predicted by device simulation. Further comments and results on large-signal analysis using the LUT approach could be found in [20].

B. Application of LUT-LF Approach

The lookup tables of $y$-parameters can be used to simulate small-signal performance of transistor circuits directly. As an example, we consider a 2.4-GHz low-noise amplifier (LNA) circuit shown schematically in Fig. 5. The lookup tables used for transistors M1 and M2 were extracted using the measurement technique described in Section II with $\Delta V_{DS} = 0.2$ V, $\Delta V_{GS} = 0.2$ V, and $\Delta V_{BS} = -0.6$ V as the grid spacings. The spiral inductors and MOM capacitors were modeled using ICCAP. For transistors in the current source circuit, BSIM3 models were used.

Two-port $y$-parameters of the LNA circuit were measured and converted into $y$-parameters. After that, a one-step deembedding was performed. The deembedded $y$-parameters are shown in Fig. 6(a) and (b) along with the simulated $y$-parameters for different bias conditions. A good agreement is found between the measured and simulated results. This example brings out the usefulness of the LUT approach for simulation of RF circuits.

IV. HIGH-FREQUENCY SMALL-SIGNAL LUT APPROACH (LUT-HF)

In the LUT-LF approach, the non-quasi-static (NQS) effects in the device as well as parasitic effects due to lead inductances...
etc. are not included. This limits the range of validity of the LUT-LF approach. Fig. 7 shows the plots of normalized error in $y$-parameters i.e., the difference between $y$-parameters measured at a given frequency and its low-frequency (0.6 GHz) value. We see that, for frequencies above 3 GHz, the error goes beyond 10%. For the 2.4-GHz LNA described in Section III, the LUT-LF approach is adequate; however, at higher operating frequencies, the LUT-LF approach would not be appropriate.

For high-frequency applications, it is clear that $y$-parameters measured at the frequency of interest must be used directly rather than values extrapolated from low-frequency measurements. At low frequencies, where NQS effects and parasitic effects are negligible, the real and imaginary parts of $y$-parameters can be shown to be independent of frequency [4]. However, at high frequencies, the frequency dependence must be accounted for by generating multiple LUTs corresponding to different frequencies. In this work, we have used steps of 0.5 GHz in the frequency axis. The dc operating bias for the device is calculated using the LUT-LF approach. For the small-signal ac analysis, the device has been modeled as a table of terminal voltages and all capacitances and conductances ($y$-parameters) of the device. The defining equations for the terminal current $I_x$ is [4]

$$I_x = \sum_{i=g,d,s,b} (a_{xi} + j\omega c_{xi}) V_i \tag{10}$$

where $x$ can be gate, drain, source, or bulk. The terms $a_{xi}$ and $c_{xi}$ are the conductance and capacitance between the nodes $x$ and $i$ of the MOS device. These quantities are bias- and frequency-dependent, and $V_i$ represents the small-signal voltage at the $i^{th}$ terminal of the four-terminal MOS device. We will call this the LUT-HF approach. Note that, a suitable interpolation scheme must be employed in this approach to compute the LUT entries at frequencies other than the measurement frequencies. This additional interpolation with respect to frequency is not required in the LUT-LF approach of Section III where the entries are independent of frequency. The LUT-HF approach thus requires more computer memory as compared to the LUT-LF approach.

A. Circuit Simulation Example: Tuned Amplifier

To illustrate the need for using the more complex LUT-HF approach, we consider a tuned amplifier circuit (inset, Fig. 8(a)) tuned at two different frequencies. This circuit was simulated using the measured MOSFET lookup tables with both LUT-LF and LUT-HF approaches. The results obtained from the two approaches are shown in Fig. 8. The results are in good agreement at a tuning frequency of 1 GHz. However, for a tuning frequency of 8 GHz, the LUT-LF results deviate significantly from the LUT-HF results. This discrepancy is expected since the LUT-LF approach does not account for frequency dependence of the $y$-parameters which, as illustrated in Fig. 7, show significant deviation beyond 3 GHz. The simulation results presented here using the measured $y$-parameters are in qualitative agreement with a more detailed study using 2-D device simulations [22].

V. CONCLUSION

We have presented a practical and accurate technique for measurement of three-port network-parameters for a MOS
transistor using two-port measurements. The measured $y$-parameters in the form of lookup tables were used for simulation of a low-noise amplifier circuit, and excellent agreement was demonstrated between the simulated and measured performance. It was emphasized that, at high frequencies, several lookup tables need to be employed, each corresponding to a different frequency, in order to predict the circuit performance accurately. The need for the LUT-HF approach was clearly demonstrated with a tuned amplifier simulation example.

REFERENCES


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