Optimization and Realization of Sub-100-nm Channel Length Single Halo p-MOSFETs

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Abstract—Single halo p-MOSFETs with channel lengths down to 100 nm are optimized, fabricated, and characterized as part of this study. We show extensive device characterization results to study the effect of large angle V_T adjust implant parameters on device performance and hot carrier reliability. Results on both conventionally doped and single halo p-MOSFETs have been presented for comparison purposes.

Index Terms—Asymmetric channel, charge-pumping, halo doping, hotcarrier, LAC, MOSFET optimization, p-MOSFET.

I. INTRODUCTION

As technology scaling is pushing device dimensions into sub-0.1 μ m regime, short channel effects and reliability issues have become areas of severe concern. Since conventional gate oxide thickness scaling gives rise to higher gate leakage, alternative approaches such as the use of channel engineering to alleviate these concerns will be a critical part of device design. Hot electron degradation, punch-through suppression, and threshold variations with channel length are some of the important issues that can be addressed with proper channel doping profile design. Single halo (SH) MOSFETs have been investigated in this respect by various researchers [1]-[6], [9], [7]. In this brief, using extensive experimental results on SH and conventional homogeneously doped channel (conventional) p-MOSFETs, we show, for the first time, that SH devices can be optimized for improved performance and reliability. We also study the effect of tilt angle of the lateral asymmetric V_T adjust implant on the transistor performance and hot-carrier reliability.

II. DEVICE FABRICATION

The schematic of the fabricated SH p-MOSFET is shown in Fig. 1 along with the doping profiles obtained using process simulator TSUPREM [8]. The SH and conventional p-MOSFETs are fabricated on both bulk and SOI wafers using E-beam lithography to define channel length down to 0.1μ m. After the gate formation, 10 keV As ions at a dose of 4×10^{14} cm⁻² are implanted with tilt angles of 7°, 10° , and 15° to realize halo doping profile in the channel region and for V_T adjustment. A Ti silicidation process with Ge preamorphization is implemented to control the silicide depth and reduce the series resistance. Annealing is done at 1000 °C for 10 min. Such a low temperature silicidation reduces the dopant redistribution, which is extremely important to realize single halo structures in 0.1 μ m channel p-MOSFETs. We have used N₂O grown oxide to suppress boron penetration problems from the p+ poly gate. The gate oxide

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1077



Fig. 1. (a) Schematic of single halo p-MOSFET structure. (b) Source/drain and channel doping profiles as obtained from TSUPREM.



Fig. 2. (a) Output characteristics of 0.1 μ m channel length SH and conventional p-MOSFETs. (b) Measured saturation transconductance as a function of channel length for the 15° tilt angle SH and conventional MOSFETs. The effect of tilt angle variation on the saturation transcoductance is shown in the inset for a 0.1 μ m channel length MOSFET.

thickness measured from C-V characteristics is 3.7 nm. Both the SH and CONV-MOSFETs are fabricated on the same wafer for realistic comparisons.

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Fig. 3. Measured hole drift velocity g_{mi} /WCox and intrinsic saturation transconductance g_{mi} as a function of channel length for 15° tilt angle SH and conventional p-MOSFETs.



Fig. 4. Lateral electric field along the channel for a single halo and conventional p-MOSFET.



Fig. 5. Peak substrate current as a function of channel length for SH and conventional p-MOSFETs (SH tilt angle was 15°).

III. ELECTRICAL CHARACTERISTICS

Fig. 2(a) shows the measured output characteristics of both SH and conventional 0.1 μ m channel length p-MOSFETs at identical gate overdrive. The SH device shows improved drive currents compared to the conventional device. Fig. 2(b) shows the saturation transconductance as a function of channel length. It can be seen that the SH devices exhibit a higher saturation transconductance compared to the conventional MOSFETs. The effect of tilt angle on the device saturation transconductance is shown in the inset of Fig. 2(b). As can be seen, with an increase in the tilt angle, the MOSFET transconductance decreases and becomes identical to the conventional uniformly doped channel MOSFETs. This is because, for lower tilt angles, the channel doping is confined to a smaller region at source side leaving



Fig. 6. (a) Charge pumping current (I_{CP}) measured as a function of V_{top} in SH and CONV p-MOSFETs. I_{CP} was measured before and after a 100 sec hot-carrier stress at the stress condition $|V_G| = |V_D|/2$, at a drain bias of -4.2 V. (b) Increase in charge pumping current (ΔI_{cp}) , due to hot carrier stress, as a function of tilt angle for 0.1 μ m channel length SH p-MOSFETs. The stressing was done at $|V_G| = |V_D|/2$, at a drain bias of -4.2 V.

an increasing portion of the channel lightly doped. This increases the average mobility in the channel that contributes to an increase in saturation transconductance. The higher peak doping near the source region also gives rise to an early velocity rise for the carriers, which leads to a higher average carrier velocity in the channel for the SH MOSFETs [7]. The measured values of average channel hole velocity, extracted from the intrinsic transconductances are shown in Fig. 3. It can be noted that the SH devices show higher average carrier velocity compared to the conventional devices. Fig. 4 shows the lateral channel electric field for conventional and SH structures. As can be seen, any increase in the electric field near the source junction is associated with a reduction in the peak electric field near the drain side, for the SH devices, which reduces the impact ionization rate for these devices. This can lead to an improved hot-carrier reliability for SH MOSFETs. Fig. 5 shows the measured substrate currents as a function of channel length for conventional and SH transistors at various negative drain biases for the p-MOSFETs. It is seen that the peak substrate current in SH MOSFETs is almost a factor of two lower compared to the conventional MOSFETs in the 0.1 μ m channel length regime. Fig. 6(a) and (b) show the pre- and poststress charge pumping (C-P) currents measured for SH p-MOSFETs with different tilt angles. The pre-stress N_{it} of these devices, as extracted from the measured C-P data, was in the low 10^{10} cm⁻² range. It can be clearly seen that the interface degradation increases with the tilt angle for the SH devices. This can be attributed to a higher peak electric field near the drain junction, which increases with increasing tilt angle.

IV. CONCLUSIONS

The experimental results presented in this paper show optimization trends for SH p-MOSFETs with various halo implantation angles. As can be seen from the experimental data, SH MOSFETs show a higher current drive and saturation transconductance, which can be attributed to an increase in the average velocity of channel carriers in these devices. It has also been shown that a decrease in the peak lateral electric field in the SH MOSFETs gives rise to an improved reliability performance, as can be seen from the measured substrate currents and interface degradation. Our results also indicate that the lower tilt angles for V_T adjust implant give rise to a better confinement of channel doping concentration near the source side, which is effective in improving the device transconductance as well as the reliability performance.

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New Collector Undercut Technique Using a SiN Sidewall for Low Base Contact Resistance in InP/InGaAs SHBTs

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Abstract—A new collector undercut process using SiN protection sidewall has been developed for high speed InP/InGaAs single heterojunction bipolar transistors (HBTs). The HBTs fabricated using the technique have a larger base contact area, resulting in a smaller DC current gain and smaller base contact resistance than HBTs fabricated using a conventional undercut process while maintaining low C_{bc} . Due to the reduced base contact resistance, the maximum oscillation frequency (f_{max}) has been enhanced from 162 GHz to 208 GHz. This result clearly shows the effectiveness of this technique for high-speed HBT process, especially for the HBTs with a thick collector layer, and narrow base metal width.

Index Terms—Base–collector capacitance, base resistance, collector undercut, heterojunction bipolar transistors (HBTs).

I. INTRODUCTION

Many research works have been devoted to reducing the base–collector capacitance (C_{bc}) and base resistance (R_b) in HBT for a high speed operation since $f_{max} = \sqrt{f_T/8\pi R_b C_{bc}}$. Ion implantation technique is the most widely used for reduced C_{bc} of GaAs HBTs, but it is not a viable technique for InP-based HBTs [1], [2]. Regrown base [3], and L-shaped base electrodes [4] are used for reduction of R_b . The transferred substrate technique, which can minimize the C_{bc} , yields an HBT with f_{max} in excess of 1 THz [5]. Simple collector undercut is the most widely used to reduce the C_{bc} of InP double-HBTs due to the selective etching nature [6]–[8]. In the case of single-HBTs, however, the base layer is also etched during the collector undercut process because the selective etch cannot be employed.

In this brief, we propose a new collector undercut technique that does not etch the base layer laterally using SiN protection sidewall. Because the base contact layer is intact during the undercut, the contact resistance is maintained low. In this process, the surfaces of the emitter sidewall and extrinsic base are passivated by polyimide [9] and a low parasitic interconnection using air-bridge is also employed. The RF performance data of the HBT clearly demonstrate the effectiveness of the new process technique.

II. DEVICE STRUCTURE AND FABRICATION

The epitaxial layer of the fabricated HBTs is grown by solid source molecular beam epitaxy (SSMBE) on a Fe-doped semi-insulating (100) InP substrate, starting with a 5000 Å InGaAs subcollector layer and 6000-Å-thick, 2.0×10^{16} cm⁻³ Si-doped collector layer. The 600 Å InGaAs base is Be-doped to 3.0×10^{19} cm⁻³ with a 70-Å undoped spacer. The emitter layer is a 1000-Å InP with Si-doped to 5.0×10^{17} cm⁻³, followed by the InGaAs cap layer. The details are outlined in Table I.

Fabrication starts with the evaporation of Ti/Pt/Au emitter contact metals. Emitter etch, which is the most delicate step, was carried out by

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