Modeling of the CoolMOS™ Transistor—Part II: DC Model and Parameter Extraction

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***Abstract*—An accurate dc model for the CoolMOS™ power transistor is presented. An elementary model consisting of an intrinsic MOSFET and a JFET to represent the drift region, is first discussed and it is pointed out that this is a rather poor model, needing improvements. Using device simulation results, it is shown that, by replacing the gate and drain voltages of the intrinsic MOSFET by appropriate "effective" voltages, a highly accurate model is obtained. A systematic procedure for parameter extraction is described and an implementation of the new model in the form of a SPICE subcircuit is given.**

***Index Terms*—CoolMOS model, CoolMOS parameter extraction, power MOSFET model.**

I. Introduction

COOLMOS™ is a novel power MOSFET [1], [2] employing a "superjunction" to sustain the voltage when the device is not conducting. The presence of the superjunction greatly improves the relationship between the on resistance and the breakdown voltage. Analytic treatment of the superjunction has been presented in [3]–[7]. In an accompanying paper [8], we have investigated the device operation in the off state and in the on state, using device simulation. The physical phenomena responsible for the higher breakdown voltage of the CoolMOS™ transistor and quasi saturation of the drain current were discussed. In the on state, it was seen that, as the drain voltage is increased, the drift region (i.e., the superjunction) gets depleted. However, the depletion region stops expanding beyond a certain point. The reasons for this were examined. It was also pointed out that the JFET-like region of CoolMOS™ is composed of a "neck" region and a "pillar" region.

It is the purpose of this paper to propose a model for the dc characteristics of the CoolMOS™ transistor. In Section II, we start with a basic model, consisting of an intrinsic MOSFET in series with a JFET and show that this model is inadequate to describe the current–voltage (I–V) characteristics. We then augment this basic model, in Section III and define "effective" drain and gate voltages to model the I–V characteristics accurately. Device simulation results for two CoolMOS™ structures are presented and it is shown that the proposed model matches the I–V characteristics very well. A variation of the proposed model is also described in the Appendix and the issues related to accuracy and parameter extraction are discussed.

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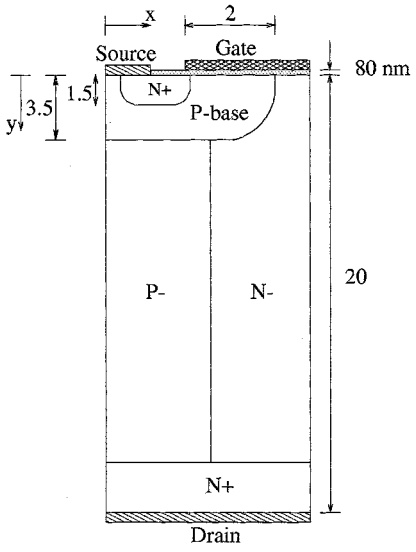

Fig. 1. Simulated CoolMOS™ structure. All dimensions are in micron unless specified otherwise. The structure shown here represents one "cell" of the device.

II. Basic Model

A simple model was first developed, based on simulation results obtained with PISCES [8]. The simulated device is shown in Fig. 1. The doping densities in the drift region were assumed to be $N_d = N_a = 1 \times 10^{16}$ cm^{-3} in the n$^-$ and p$^-$ strips. The main observations related to circuit modeling were the following [8]. a) For low gate voltages, the current saturates at high V_D, due to the saturation of the "intrinsic" MOSFET and b) At higher gate voltages, the I_D–V_D characteristics show "quasi-saturation," which is a result of velocity saturation in the n$^-$ drift region. Quasi-saturation has also been observed in VDMOSTs [9]. In this paper, we will assume that V_G is not high enough for quasi saturation to occur. As quasi-saturation is a degrading effect, practical devices are designed to avoid it anyway. c) The depletion region behavior in the drift region is similar to that in a JFET. Physically, the drift region behavior suggests a model with two JFETs in series, one for the "neck" region and the other for the "pillar" region. Analytical modeling of the "pillar" part of the drift region was also done in [8], which confirmed that its I–V equation is similar to that of a JFET.

The structure of the CoolMOS™ transistor and simulation results described in [8] suggest a basic model for the CoolMOS™ device consisting of an intrinsic MOSFET in

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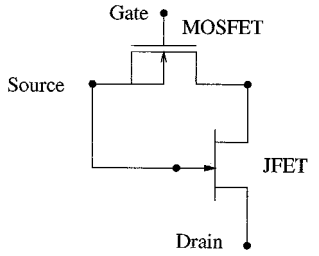

Fig. 2. Basic CoolMOS™ model.

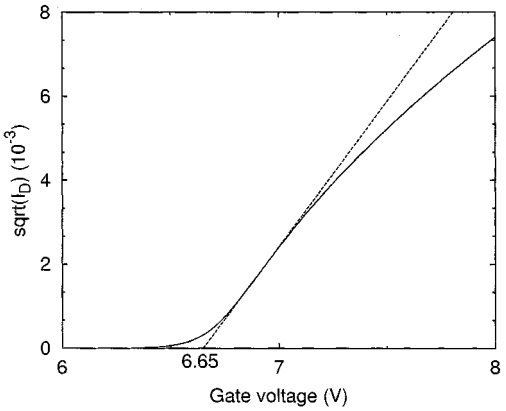

Fig. 3. $\sqrt{I_D}$ versus V_G at $V_D = 25$ V. The solid line shows the PISCES result and the dashed line is the straight line fit.

series with a "neck" JFET, followed by the "pillar" JFET. Existing VDMOST circuit models are based on a similar framework [10]–[12], with the drift region represented by either a resistor, or by a resistor in series with a JFET, the latter being structurally more suitable. For the CoolMOS™ device, using two JFETs for the drift region makes parameter extraction extremely difficult, as we will discuss in the Appendix. Hence, a simpler model consisting of a MOSFET in series with a JFET (see Fig. 2) was first considered. In effect, we are combining the action of two JFETs into one equivalent JFET.

The SPICE level 3 MOSFET model, which requires primarily the two parameters V_T and K_p, was used for the intrinsic MOSFET. The parameters are obtained from the transfer characteristics at high V_D (25 V in this case). The tangent drawn at the point of maximum slope of the $\sqrt{I_D}$ versus V_G curve has an intercept equal to V_T and a slope equal to $\sqrt{K_p/2}$. For the simulated device, this plot is shown in Fig. 3 and it gives $V_T = 6.65$ V and $K_p = 1.1 \times 10^{-4}$ A/V^2. Note that the current obtained with PISCES is actually current per unit width (i.e., 1 μm). To be precise, we must treat the current to be in Amp/μm. For simplicity, however, we will denote it simply as Amp. For a device width different from 1 μm, the current will simply change proportionately.

The commonly used technique of finding V_T and K_p from the low-V_D I_D-V_G curve was not preferred here, since the resistance of the drift region causes the voltage at the intrinsic MOSFET drain to reduce with current. This was estimated to produce an error of more than 50% in the slope.

For the JFET part of the model (see Fig. 2) in SPICE, two parameters (V_T and β) are required. The current prior to pinch off is given by

$$I_D = \beta V_{DS} \left[2 \left(V_{GS} - V_T \right) - V_{DS} \right] \tag{1}$$

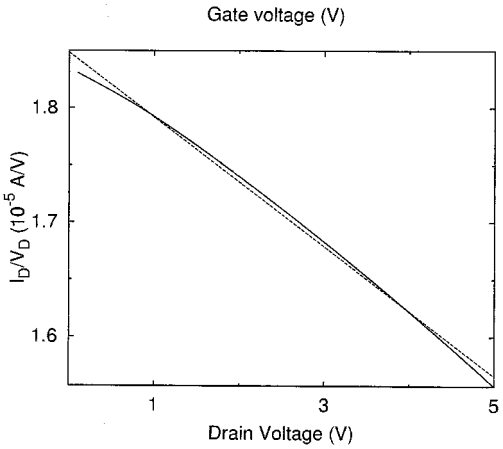

Fig. 4. I_D–V_D versus V_D at $V_G = 40$ V. The solid line indicates the PISCES result, and the dashed line shows a straight line fit.

where $V_T = -V_p$, V_p being the pinch-off voltage. For $V_{GS} = 0$ V and defining a resistance $R = V_{DS}/I$, we get

$$\frac{1}{R} = \beta \left(2V_P - V_{DS} \right). \tag{2}$$

Note that for the JFET, the drain is the same as the drain of the CoolMOS™ transistor (see Fig. 1) and the source corresponds to the drain of the intrinsic MOSFET. The CoolMOS™ source acts like the gate of the JFET, as its potential is nearly the same as that in the neutral part of the p$^-$ strip. If the CoolMOS™ V_G is high, the resistance of the MOSFET channel is small and we may assume that the entire V_{DS} of the CoolMOS™ transistor appears as V_{DS} of the JFET. Thus, if we make V_G of the CoolMOS™ transistor large (assuming the source to be grounded), it would ensure that $V_{DS} \simeq V_D$ and $V_{GS} \simeq 0$ V for the JFET. We can then use (2), which suggests that a plot of $1/R$ versus V_D would yield the parameters V_p and β of the JFET.

Fig. 4 shows I_D versus V_D, as obtained from PISCES, for the CoolMOS™ structure (Fig. 1) for a large V_G. Also shown in the figure is a straight line fit from which, using (2), the parameters for the JFET were found to be $V_p = 16.3$ V and $\beta = 5.7 \times 10^{-7}$ A/V^2.

Using the MOSFET and JFET parameters extracted as described earlier, I–V characteristics were obtained with SPICE. Fig. 5 shows two of the characteristics along with the PISCES results. The agreement between the two is clearly not satisfactory.

III. Improvements in the Basic Model

The simple model described in Section II obviously needs improvement. In fact, we could have *expected* the simple model to be inadequate, as it does not take into account the following complications. i) In the intrinsic MOSFET, the channel doping density is not uniform, as the channel region is actually formed by diffusion. This makes the validity of the SPICE level 3 model questionable. ii) In Section II, we have referred to the "drain" of the intrinsic MOSFET as if it is a known point is space. In reality, however, the situation is made more complicated by the two-dimensional nature of the problem and it is not always possible to treat a fixed point as the drain of the intrinsic MOSFET. iii)

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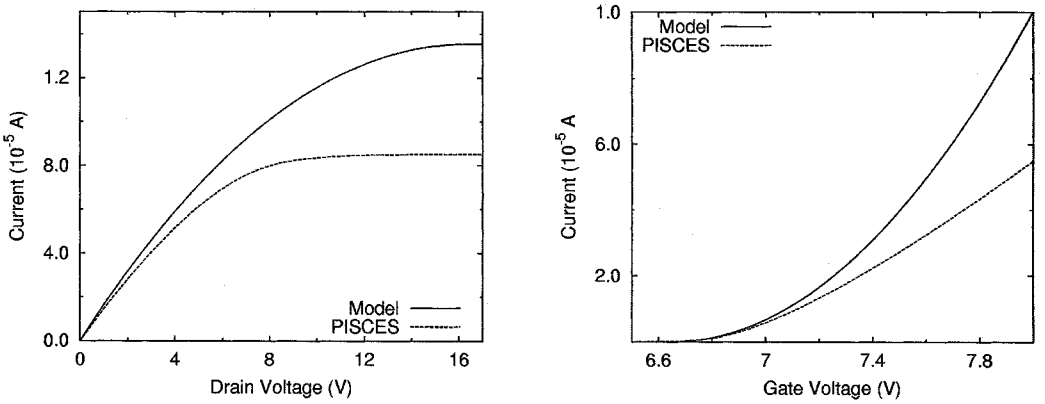

Fig. 5. I–V characteristics obtained with the basic model and with PISCES.

The effects of velocity saturation/mobility degradation have not been explicitly included in the model. iv) As discussed in [8], a more accurate representation of the drift region would involve two JFETs in series, one for the "neck" region and the other for the "pillar" region.

Clearly, the aforementioned complex physical phenomena are not easy to model. Further, if a model is developed successfully to account for all of the above second-order effects, it is likely to be very complicated and difficult to implement in a circuit simulator. We have therefore adopted a somewhat empirical approach to improve the basic model of Section II. A systematic procedure to extract all of the model parameters, using I_D–V_G and I_D-V_D characteristics, will emerge from the following discussion.

Let us begin with the relationship between I_D and V_G for an ideal MOSFET in saturation, viz.

$$I_D = \frac{K_p}{2}(V_G - V_T)^2, \text{ or} \tag{3}$$

$$(V_G - V_T) = \sqrt{\frac{2I_D}{K_p}}. \tag{4}$$

Now, from Fig. 5(b), we see that our simple model of Section II, which follows (4), overestimates the drain current in the saturation region. In other words, the actual values of V_G and I_D (the lower curve in [Fig. 5(b)]) do not satisfy (4). Let us now define an "effective" gate voltage $V_{G\text{eff}}$ which will satisfy (4), i.e.,

$$(V_{G\text{eff}} - V_T) = \sqrt{\frac{2I_D}{K_p}}. \tag{5}$$

Equation (5) can be rewritten in the form

$$V_G - V_{G\text{eff}} = (V_G - V_T) - \sqrt{\frac{2I_D}{K_p}}. \tag{6}$$

If we place a voltage source (of magnitude $V_G - V_{G\text{eff}}$) between the gate of CoolMOS™ and the gate of the intrinsic MOS transistor, it is equivalent to applying a gate voltage $V_{G\text{eff}}$ to the intrinsic MOSFET, which will then produce the correct value of I_D. This is the motivation behind defining $V_{G\text{eff}}$. The next step is to find out how $V_{G\text{eff}}$ varies with V_G and to model it appropriately.

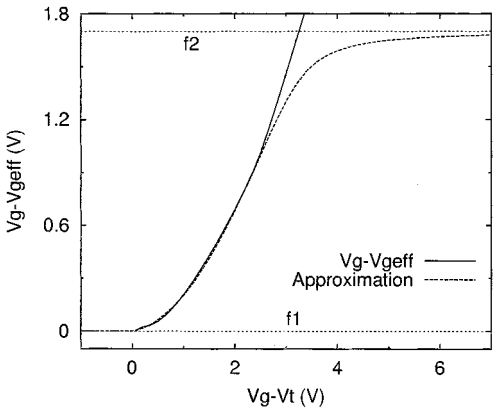

Fig. 6. $(V_G - V_{G\text{eff}})$ versus $(V_G - V_T)$ as obtained with PISCES (solid line) and the approximated $(V_G - V_{G\text{eff}})$ (dashed line). The horizontal lines marked $f1$ and $f2$ indicate $(V_G - V_{G\text{eff}}) = 0$ V and 1.7 V, respectively.

Fig. 6 shows $(V_G - V_{G\text{eff}})$ versus $(V_G - V_T)$, as obtained from the PISCES results [Fig. 5(b)]. Our first goal is to fit this function suitably, which we do with a cubic polynomial in $(V_G - V_T)$. Note that, at higher gate voltages, (say, $(V_G - V_T) > 3$ V in this case), the MOSFET comes out of saturation [8] and the drain current is determined by the JFET. Thus, the exact value of $(V_G - V_{G\text{eff}})$ is not important at high values of V_G; we have chosen to make $(V_G - V_{G\text{eff}})$ approach a constant value (about 1.7 V, see Fig. 6), as V_G becomes large. This is achieved by using a function f [13]

$$f(g(x)) = g_{\max} - \frac{1}{2}\Big(g_{\max} - g(x) - \delta + \sqrt{(g_{\max} - g(x) - \delta)^2 + 4\delta g_{\max}}\Big) \tag{7}$$

where $g_{\max}$ is the maximum value of $g(x) \equiv (V_G - V_{G\text{eff}})$ that we want to enforce. The smoothness of this function f is controlled by the parameter δ [13]. The resulting function f is shown in Fig. 6 as the dashed line.

The deviation of the I_D–V_G characteristic from the expected quadratic relationship may be explained qualitatively in terms of the nonuniform doping denisty in the MOSFET channel. Let us illustrate this by considering a hypothetical MOS transistor with two distinct doping densities in the channel region: N_{AS} near the source and N_{AD} near the drain, where $N_{AS} > N_{AD}$. Let us denote the corresponding threshold voltages by V_{TS} and V_{TD},

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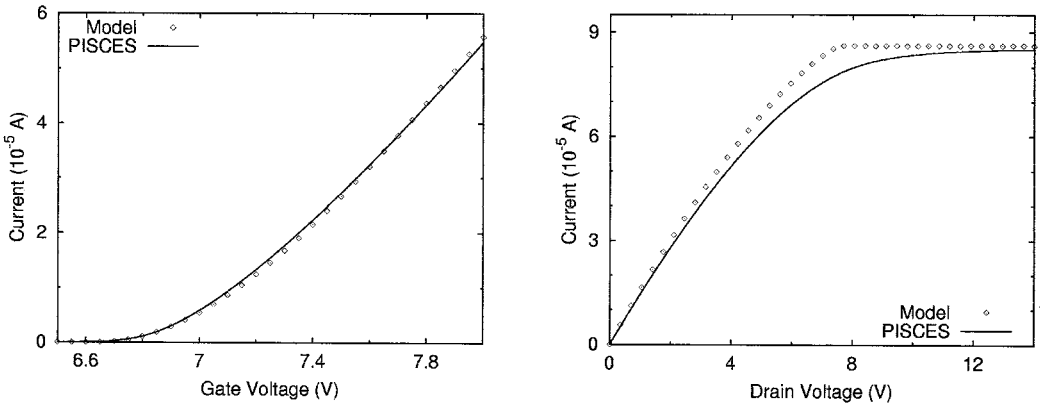

Fig. 7. I–V characteristics for the CoolMOS™ transistor: PISCES results (line) and model results (symbols). The model consists of the basic model of Fig. 2, with V_G replaced with $V_{G\text{eff}}$.

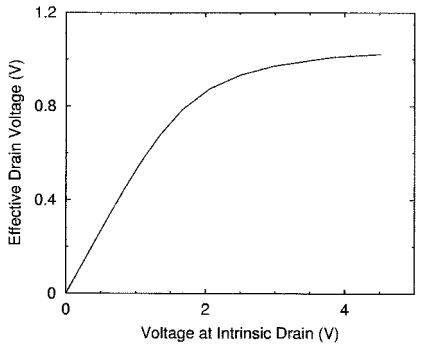

Fig. 8. Effective drain voltage ($V^i_{D\text{eff}}$) versus the drain voltage of the intrinsic MOSFET (V^i_D) as obtained from the PISCES results.

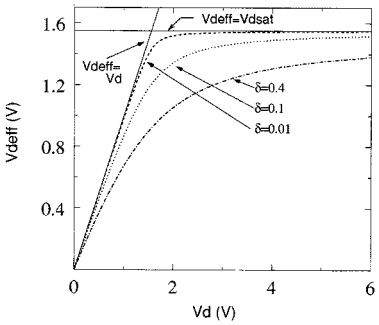

Fig. 9. Approximation for $V^i_{D\text{eff}}$ versus V^i_D for various values of δ. The two asymptotes, $V^i_{D\text{eff}} = V^i_D$ and $V^i_{D\text{eff}} = V_{D\text{sat}}$, are also shown.

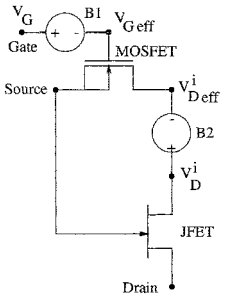

Fig. 10. Complete on-state dc model for the CoolMOS™ transistor.

```
MOSFET 2 3 1 1 model1
JFET 5 1 4 model2
VG 6 0 dc
VS 1 0 dc
VD 5 0 dc
B1a 10 0 v = v(6)-6.65
B1b 11 0 v = -1*(5.31-02*v(10)+
+  1.64e-01*(v(10)\^2)-3.38e-03*(v(10)\^3))
B1c 12 0 v = 0.5*(0-v(11)-0.001+
+  sqrt((0-v(11)-0.001)\^2))
B2a 13 0 v = 0.5*(v(3)-6.65-0.01+
+  sqrt((v(3)-6.65-0.01)\^2))
B1 6 3 v = 1.7-0.5*(1.7-v(12)-0.07+
+  sqrt((1.7-v(12)-0.07)\^2+4*0.07*1.7))
B2 4 2 v = v(4)-v(13)+0.5*(v(13)-v(4)-0.4+
+  sqrt((v(13)-v(4)-0.4)\^2+4*0.4*v(10)))
.model model1 nmos (level=3 vto=6.65 kp=11e-5)
.model model2 njf (vto=-16.33 beta=5.66e-7)
```

Fig. 11. SPICE subcircuit to implement the CoolMOS™ model of Fig. 10.

respectively. If we measure the threshold voltage of this MOS transistor V_T by some means, we will be actually measuring V_{TS}, the larger of the two threshold voltages. Now consider the I_D–V_G curve for a typical MOS transistor. If the transistor is in saturation, this relationship is quadratic. However, if the transistor operates in the linear regime, then I_D will deviate from the quadratic. For the MOSFET to leave saturation, the condition is $V_{DS} < V_{GS} - V_T$. Note that V_T in this condition is the value of V_T near the drain, i.e., V_{TD}. In other words, the device will come out of saturation (for a constant V_{DS}) at a lower value of V_{GS}. Hence we can expect the I_D–V_G curve to fall below the quadratic at an earlier stage, than we would expect on the basis of the measured threshold voltage, i.e., V_{TS}. Specifically, the actual drain current will be *less* than the expected current, as seen in Fig. 5(b). Our definition of $V_{G\text{eff}}$ is basically a way to indirectly model this complex I_D–V_G relationship.

This improvement, viz., application of $V_{G\text{eff}}$ to the gate of the intrinsic MOSFET (instead of V_G) was incorporated in the basic model of Fig. 2. As expected, the I_D–V_G characteristics for large V_D now match well with the PISCES results [Fig. 7(a)]; however, the I_D-V_D characteristics need further improvement [Fig. 7(b)]. This brings us to the second modification of the basic model of Fig. 2. Let us illustrate this modification with an example.

Suppose we apply a constant $V_G = 8.5$ V to the CoolMOS™ transistor and obtain I_D as a function of V_D with PISCES. The terminal voltage V_D is, of course, different from the *intrinsic* drain voltage of the MOSFET. Let us denote this intrinsic voltage by V^i_D. From PISCES simulation results, we can extract the value of V^i_D for each V_D. Now, using our basic model (with V_G replaced by $V_{G\text{eff}}$ as discussed earlier), we compute an *effective* intrinsic drain voltage ($V^i_{D\text{eff}}$), which will result in the same drain current as the PISCES result. In Fig. 8, we have plotted

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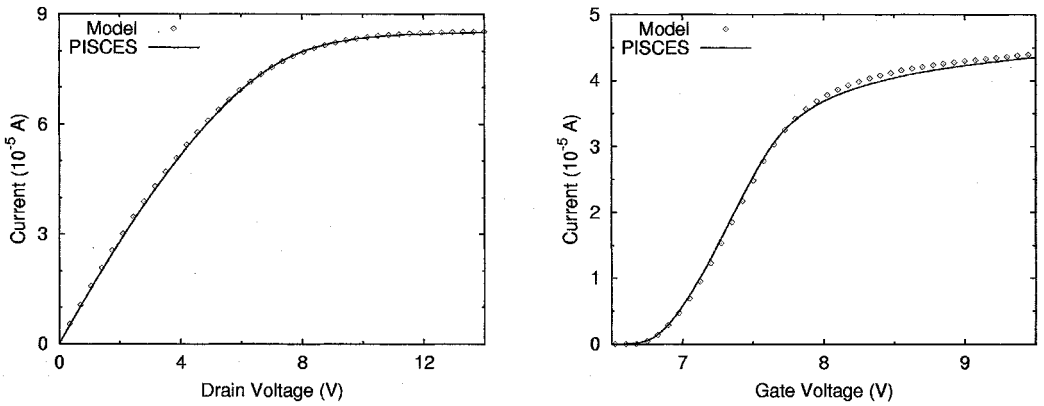

Fig. 12. I–V characteristics for the CoolMOS™ transistor: PISCES results (line) and model results (symbols). The model consists of the basic model of Fig. 2, with V_G replaced with $V_{G\text{eff}}$ and V_D^i replaced with $V_{D\text{eff}}^i$.

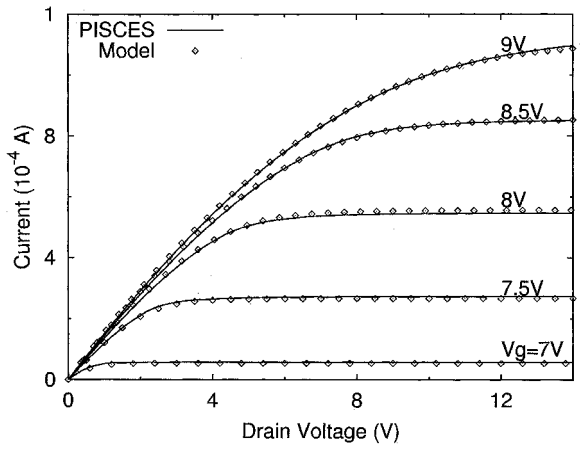

Fig. 13. I_D-V_D characteristics for the CoolMOS™ structure of Fig. 1: PISCES results (lines) and model results (symbols).

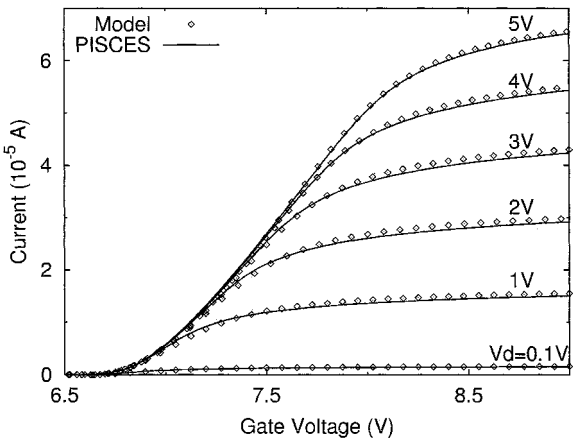

Fig. 14. I_D–V_G characteristics for the CoolMOS™ structure of Fig. 1: PISCES results (lines) and model results (symbols).

$V_{D\text{eff}}^i$ so obtained as a function of V_D^i. This idea is not new; it has already been incorporated in the BSIM3 MOS transistor model [13].

The relationship between $V_{D\text{eff}}^i$ and V_D^i of Fig. 8 can be approximated using two asymptotes (see Fig. 9) and then using the function described by (7) with appropriate changes. Fig. 9 shows the effect of varying the parameter δ on the $V_{D\text{eff}}^i$ versus V_D^i relationship. In practice, of course, we do not have access to the intrinsic drain voltage; thus, we cannot extract the value of δ using the procedure mentioned earlier. We will therefore treat δ simply as a fitting parameter.

The previous modification of the basic model can be incorporated by adding a suitable dependent source "B2" between the drain of the intrinsic MOSFET and the source of the JFET, as shown in Fig. 10. The dependent source "B1" in Fig. 10 represents $(V_G - V_{G\text{eff}})$ as we have seen earlier. A SPICE subcircuit to implement the complete model of Fig. 10 is given in Fig. 11.

The effect of the second modification of the basic model (i.e., that of the source B2) is immediately apparent in the characteristics shown in Fig. 12. Both the I_D-V_D and I_D–V_G curve at a low V_D are now accurately reproduced by the model. The I_D–V_G curve at high V_D [Fig. 7(a)] is not affected by B2 and is therefore not shown again.

In Figs. 13 and 14, a family of I_D-V_D and I_D–V_G curves for CoolMOS™ are plotted. It is seen that the model shows excellent agreement with the simulation results. To verify the generality of the model, another CoolMOS™ structure was simulated, with a different geometry, channel doping density, and channel length. This new structure had drift region strips of height 25 μm and width 2 μm and a channel length of 1.5 μm. The model parameters were extracted from the simulation results and I–V characteristics were computed. Again, an excellent agreement between the model and simulation results was obtained (Figs. 15 and 16).

In reality, the sources B1 and B2 of Fig. 10 seem to have no "physical" counterpart in the device. The definitions of $V_{G\text{eff}}$ and $V_{D\text{eff}}^i$ can be thought of as "lumping" of the second-order effects discussed earlier into effective bias voltages. However, the proposed model is clearly attractive from the circuit simulation point of view, as it can be implemented as a simple SPICE subcircuit.

APPENDIX

Before formulating the CoolMOS™ model of Section III, we tried out what appears to be a more accurate approach. However, some difficulties were encountered and this approach was not pursued further. It is the purpose of this Appendix to discuss these issues.

As we have shown in [8], the JFET-type region of the CoolMOS™ device is composed of two regions: the "neck"

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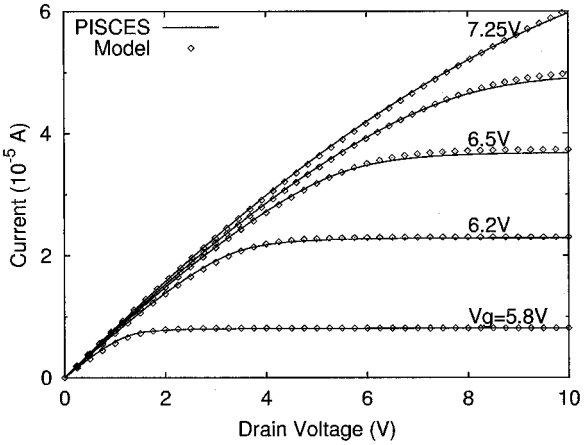

Fig. 15. I_D-V_D characteristics for the CoolMOS™ structure of Fig. 1, but with different dimensions and doping densities (see text): PISCES results (lines) and model results (symbols).

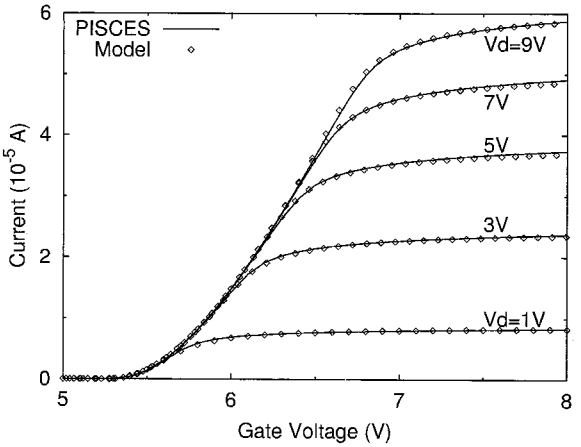

Fig. 16. I_D–V_G characteristics for the CoolMOS™ structure of Fig. 1, but with different dimensions and doping densities (see text): PISCES results (lines) and model results (symbols).

region and the "pillar" region. If we denote the total resistance of the drift region as R_J, then $R_J = R_{Jn} + R_{Jp}$, where R_{Jn} corresponds to the resistance of the neck region and R_{Jp} to that of the pillar region. For low values of V_{DS} (i.e., the JFETs in the linear region) $R_{Jn} = 1/\beta_n V_{Pn}$ and $R_{Jp} = 1/\beta_p V_{Pp}$. Let us define $k = R_{Jn}/(R_{Jn} + R_{Jp})$. We will make the following assumptions. i) $k \ll 1$, i.e., the resistance of the pillar region, is much higher than that of the neck region. ii) The ratio R_{Jn}/R_{Jp} is nearly constant until the neck JFET pinches off. This assumption was seen to be valid from PISCES simulation results.

If we denote as V_{Da}, the applied drain voltage at which the neck JFET pinches off, we have $V_{Pn} = kV_{Da}$ from the previous assumption. Beyond pinch-off

$$R_{J_n} = \frac{1}{\beta_n \left(2V_{P_n} - V_{DS_n}\right)} = \frac{R_n}{2\left(1 - \frac{V_D}{2V_{D_a}}\right)}. \tag{8}$$

The resistance of the pillar JFET beyond pinch-off is

$$R_{J_p} = \frac{1}{\beta_p \left[2\left(V_{P_p} - kV_D\right) - (1-k)V_D\right]} \simeq \frac{R_p}{2\left(1 - \frac{V_D}{2V_{P_p}}\right)}. \tag{9}$$

From (8) and (9) and using binomial expansion, we get the following approximate relationship for R_J:

$$R_J = \frac{R_p}{2}\left(1 + \frac{V_D}{2V_{D_a}} + \frac{V_D^2}{4V_{D_a}^2}\right) + \frac{R_n}{2}\left(1 + \frac{V_D}{2V_{P_p}} + \frac{V_D^2}{4V_{P_p}^2}\right). \tag{10}$$

The parameters R_n, R_p, and V_{Pp} can be obtained from the coefficients of a quadratic fit to the R_J–V_D curve. The other JFET parameters can then be calculated as $V_{Pn} = kV_{Da}$, $\beta_n = 1/R_n V_{Pn}$, and $\beta_p = 1/R_p V_{Pp}$. However, we found that this method was not a robust one for the following reasons. i) The exact voltage V_{Da}, at which the neck JFET pinches off, is not easy to establish. A small error in this value results in considerably different sets of parameters. ii) The assumptions and approximations made here may not hold for a wide range of device dimensions and doping densities. For these reasons, we could not pursue this model further.

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