# Using Soft Secondary Electron Programming to Reduce Drain Disturb in Floating-Gate NOR Flash EEPROMs

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Abstract—A novel concept of soft secondary electron programming (SSEP) is introduced and shown to be a promising programming scheme for scaled NOR flash electrically erasable programmable read-only memories. Although the mechanism is similar to that of the channel-initiated secondary electron (CHISEL) programming, SSEP uses an "optimum" substrate bias that results in a lower drain disturb compared with both channel hot electron (CHE) and conventional CHISEL programming schemes. The concept behind minimizing drain disturb is discussed. SSEP is shown to give faster programming and lower disturb than CHE at all operating conditions, as well as better program/disturb margin compared with conventional CHISEL programming at similar program speed or disturb time. The effect of repeated program/erase cycling using SSEP is compared against CHE and CHISEL cycling.

*Index Terms*—Band-to-band tunneling, channel hot electron (CHE), channel-initiated secondary electron (CHISEL), cycling endurance, drain disturb, flash electrically erasable programmable read-only memory (EEPROM), secondary electrons.

## I. INTRODUCTION

LASH MEMORY market has been growing explosively with the ever increasing of with the ever increasing demand for high-density, highspeed, and low-cost nonvolatile memories [1]. One of the industry-standard flash electrically erasable programmable read-only memories (EEPROMs) is the common-ground NOR flash EEPROM that is suitable for both code and data storage applications [1], [2]. NOR flash EEPROM is a metal-oxidesemiconductor (MOS) transistor with a floating gate (FG) that is normally programmed (raise the threshold voltage  $[V_{TH}]$  by injecting electrons into the FG) using the channel hot-electron (CHE) injection and erased (lower the  $V_{\rm TH}$ ) using the uniform Fowler-Nordheim tunneling. CHE utilizes large drain and gate voltages, respectively, to heat the channel electrons and provide a favorable oxide field for their injection into the FG [3]. Apart from needing high voltages and large currents, CHE also suffers from a poor control over cell  $V_{\rm TH}$  [3], [4]. Programming using the channel-initiated secondary electron (CHISEL) injection overcomes these limitations and provides other advantages [4]–[14]. CHISEL relies on the impact ionization (II) feedback, which is activated by using a negative substrate bias during the program [11]–[14]. Here, the holes generated from the II of channel electrons are heated in the large vertical field (due to  $V_{\rm B}$ ) of drain–substrate junction (DSJ) and cause further II. The generated secondary electrons gain energy in the DSJ vertical field and are injected into the FG.

The secondary electrons in CHISEL have high energies and are injected over a spatially broader region, thereby enhancing programming efficiency [5], [15]. Compared with CHE, CHISEL offers faster program speed under equivalent power, lower power consumption under similar speed, better cycling endurance of  $V_{\rm TH}$  window, and lower degradation of program time  $T_{\rm P}$  [6], [9], [10], [16], [17]. CHISEL also leads to a selfconvergent programming, giving a better control over program  $V_{\rm TH}$  [4], [6], [11].

However, the large fields present across the drain junction under CHISEL operation are shown to give much higher program drain disturb compared with CHE operation [17], [18]. Program drain disturb is one of the serious reliability concerns of NOR flash EEPROMs that causes  $V_{\rm TH}$  shift in drain stressed cells (cells sharing the same bit line as the cell being programmed but having an unselected word line) [1], [19]. CHE drain disturb originates from subthreshold channel leakage [2] and worsens when  $L_{\rm FG}$  is scaled, whereas CHISEL drain disturb originates from band-to-band-tunneling (BTBT) at drain junction [10], [20] and worsens when source–drain (S/D) junction depth  $(X_{\rm J})$  is scaled. Hence, drain disturb can be a serious concern with cell scaling.

In this paper, we introduce the concept of using soft secondary electrons for programming, which also minimizes drain disturb. From a programming perspective, SSEP operates midway between CHE and CHISEL and is distinguished by the fact that it uses an optimum  $V_{\rm B}$  determined by minimization of drain disturb rather than by maximization of programming efficiency, which has been the case with conventional CHISEL. As a consequence, SSEP offers 1) improved disturb immunity and better program/disturb margin compared with both CHISEL and CHE and 2) better programming efficiency compared with CHE due to the presence of  $V_{\rm B}$ . The objective of this paper is to demonstrate and validate the concept of SSEP. This is an enhanced version of the work presented in [21], with the addition of results on program/erase (P/E) cycling endurance and discussion on post-cycling disturb.

Initial studies on the effect of  $V_{\rm B}$  show the presence of two competing mechanisms behind the charge gain drain disturb (CGD), namely, channel leakage and BTBT. The optimization of  $V_{\rm B}$  for SSEP involves reducing both channel leakage

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 $\sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{i=1}^{n} \sum_{i$ 

Fig. 1. Programming transients of an FG cell at different  $V_{\rm B}$  but identical  $V_{\rm CG}$  and  $V_{\rm D}$ . Programming speed increases monotonously with increasing  $|V_{\rm B}|$  due to larger number of high-energy secondary electrons.

and BTBT during disturb. We show that through proper choice of  $V_{\rm D}$ , SSEP can provide better program/disturb margin compared with CHISEL at either similar program or similar disturb performance. SSEP not only continues to give better program/ disturb performance even after repetitive P/E cycling but also shows less cycling-induced degradation compared with conventional CHISEL or CHE operation. Finally, we study the effect of scaling channel length ( $L_{\rm FG}$ ) and S/D junction depth ( $X_{\rm J}$ ) on SSEP.

## **II. EXPERIMENTAL DETAILS**

Measurements were performed on isolated FG cells with  $W = 0.30 \,\mu\text{m}, L_{\text{FG}}$  ranging from 0.22 to 0.30  $\mu\text{m}$ , tunnel oxide thickness of 12 nm, oxide-nitride-oxide (ONO) interpoly dielectric thickness of 20 nm, S/D junction depth of about 80 nm, and fabricated using a 0.18- $\mu$ m process. Programming was done using different combinations of  $V_{\rm CG}$  and  $V_{\rm D}$ , with  $V_{\rm B}$ ranging from 0 V for CHE to -2 V for CHISEL and source grounded (the optimal  $V_{\rm B}$  for CHISEL is -2 V for these cells, and CHISEL always refers to this  $V_{\rm B}$  through the rest of this paper). Erase was always done using uniform channel erase with  $V_{\rm CG} = -20$  V (source, drain, and substrate grounded). Cell  $V_{\rm TH}$  is defined using a constant current of  $I_{\rm D} = 5 \ \mu A$  at  $V_{\rm D} = 0.8$  V. Program and erase  $V_{\rm TH}$  were fixed at 5.5 and 2 V, respectively. Drain disturb (henceforth referred to as disturb) was measured at identical  $V_{\rm D}$  and  $V_{\rm B}$  during programming but with control gate grounded. Program time  $(T_{\rm P})$  and disturb time  $(T_{\rm D})$  are defined as the times needed to obtain  $V_{\rm TH}$  shifts of 3.5 and 0.1 V during program and disturb, respectively.

## **III. RESULTS AND DISCUSSION**

## A. Effect of Substrate Bias on Program and Drain Disturb

The typical dependence of programming transients on  $V_{\rm B}$  is shown in Fig. 1, with  $V_{\rm CG}$  and  $V_{\rm D}$  fixed. As is well known, programming speed increases with  $|V_{\rm B}|$  due to the increase in secondary II and the heating of secondary electrons (CHISEL principle). This continual increase in the programming speed



Fig. 2.  $T_{\rm P}$  variation with  $V_{\rm D}$  for a cell programmed at different  $V_{\rm B}$  but constant  $V_{\rm CG}$ .  $T_{\rm P}$  decreases (faster programming) with increasing  $V_{\rm D}$  and  $|V_{\rm B}|$  at all values of  $V_{\rm B}$  and  $V_{\rm D}$ , respectively.



Fig. 3. Charge gain (in erased state) and charge loss (in programmed state) drain disturb transients at different  $V_{\rm B}$ . CGD is much larger than charge loss disturb and also varies nonmonotonously with  $V_{\rm B}$ .

with increasing  $|V_{\rm B}|$  occurs at any  $V_{\rm CG}$  or  $V_{\rm D}$ .  $T_{\rm P}$  also reduces drastically at higher  $V_{\rm D}$  (for any  $V_{\rm B}$ ), which is due to the increase in both primary and secondary II. Fig. 2 shows  $T_{\rm P}$  as a function of  $V_{\rm D}$  for different  $V_{\rm B}$  at a constant  $V_{\rm CG}$ . However, it should also be noted that programming using the secondary electrons is a self-limiting process, where the maximum  $V_{\rm TH}$ attainable is limited by  $V_{\rm CG}$  [6].

Fig. 3 shows the charge gain (in erase state) and the charge loss (in program state) disturb transients at different  $V_{\rm B}$  but identical  $V_{\rm D}$ . Charge loss disturb increases with  $|V_{\rm B}|$  but is much less than CGD and is therefore not a concern. CGD, which is a real concern due to its much larger magnitude, does not vary monotonously with  $V_{\rm B}$  but is minimum at an intermediate  $V_{\rm B}$  between 0 and -2 V. This is a very important observation and is explained below.

CGD is shown to be due to hot-electron injection into the FG, with the source of hot electrons being different for CHE and CHISEL operations [20]. The sources behind CGD are shown to be channel leakage (drain-induced turn-on) and BTBT under CHE and CHISEL operations, respectively. BTBT component is insignificant in CHE operation due to lower DSJ field at  $V_{\rm B} = 0$  V, and channel leakage reduces in CHISEL operation due to body-effect ( $V_{\rm B} < 0$  V) induced  $V_{\rm TH}$  shift. Hence,



Fig. 4.  $T_{\rm D}$  (CGD) as a function of  $V_{\rm B}$  for disturb at different  $V_{\rm D}$ . Disturb is minimum near an intermediate  $V_{\rm B} = -0.8$  V independent of  $V_{\rm D}$ .



Fig. 5.  $I_{\rm B}$  during CGD as a function of  $V_{\rm B}$  at different  $V_{\rm D}$ .  $I_{\rm B}$  during disturb correlates well with  $1/T_{\rm D}$ .  $I_{\rm B}$  with floating source (no channel leakage) indicates that channel leakage is dominant at low  $|V_{\rm B}|$ , whereas BTBT is dominant at high  $|V_{\rm B}|$ .

both channel leakage and BTBT reduce at an intermediate  $V_{\rm B}$  ( $0 < |V_{\rm B}| < 2$  V), resulting in a lower drain disturb observed in Fig. 3.

Fig. 4 plots  $T_{\rm D}$  as a function of  $V_{\rm B}$  at different  $V_{\rm D}$  and shows minimum disturb (maximum  $T_{\rm D}$ ) at an intermediate  $V_{\rm B}$  between 0 and -2 V, which is independent of  $V_{\rm D}$ .  $I_{\rm B}$ during disturb is a good indicator of disturb under both CHE and CHISEL operations, as both channel leakage (through II) and BTBT contribute to  $I_{\rm B}$ . Fig. 5 plots  $I_{\rm B}$  during disturb as a function of  $V_{\rm B}$  for different  $V_{\rm D}$ , and  $I_{\rm B}$  shows a good correlation with  $1/T_{\rm D}$ . Fig. 5 also shows  $I_{\rm B}$  measured with a floating source terminal (no channel leakage), which matches with overall  $I_{\rm B}$  at high  $|V_{\rm B}|$  but is much lower at low  $|V_{\rm B}|$ . This proves that  $I_{\rm B}$  (and disturb) is mainly due to BTBT at high  $|V_{\rm B}|$ , channel leakage at low  $|V_{\rm B}|$ , and both of these at intermediate  $V_{\rm B}$ . Minimum of  $I_{\rm B}$  (minimum disturb or maximum  $T_{\rm D}$ ) occurs when  $|V_{\rm B}|$  is sufficient to reduce channel leakage but is not high enough to cause significant BTBT. Operating a cell near this bias condition is termed as SSEP, and this results in a minimum disturb that is lesser than both CHE and CHISEL conditions. Although the use of softer secondary electrons reduces the program speed compared with CHISEL, the larger improvement in  $T_{\rm D}$  is shown to give a higher program/disturb margin  $(T_{\rm D}/T_{\rm P})$ 



Fig. 6. P/E cycling characteristics of identical cells programmed using CHISEL (point a), SSEP (point b), and CHE (having the same  $V_{\rm D}$  as SSEP) operations. Program  $V_{\rm TH}$  degradation under SSEP is slightly higher than in CHISEL but comparable to CHE.



Fig. 7. Disturb transients under different conditions before and after the P/E cycling (Fig. 6). Although the disturb becomes worse with P/E cycling in all the cases, SSEP cell continues to show a much lower disturb even after cycling.

under suitable bias conditions. This optimization of  $(T_{\rm D}/T_{\rm P})$  using SSEP is discussed below.

## B. SSEP

The  $V_{\rm B}$  used for SSEP in this case is chosen to be -0.8 V (from Fig. 4), independent of  $V_{\rm D}$ . Figs. 2 and 4 (showing  $T_{\rm P}$  and  $T_{\rm D}$ , respectively) compare a CHISEL operating point "a"  $(V_{\rm D}/V_{\rm B} = 3.5/-2$  V) with two SSEP operating points "b"  $(V_{\rm D}/V_{\rm B} = 3.9/-0.8$  V) and "c"  $(V_{\rm D}/V_{\rm B} = 4.1/-0.8$  V). A  $T_{\rm P}$  of about 3  $\mu$ s can be obtained using the CHISEL point "a" or the SSEP point "b" having a slightly higher  $V_{\rm D}$  (Fig. 2). However, the resulting  $T_{\rm D}$  is an order of magnitude higher for SSEP (Fig. 4). Alternatively, comparison between the CHISEL point "a" and the SSEP point "c" having similar  $T_{\rm D}$  (Fig. 4) shows faster  $T_{\rm P}$  for SSEP (approximately twice; Fig. 2). Therefore, SSEP offers much better program/disturb margin compared with CHISEL for similar  $T_{\rm P}$  as well as similar  $T_{\rm D}$ . Furthermore, SSEP shows faster  $T_{\rm P}$  and lower  $T_{\rm D}$  compared with CHE for all  $V_{\rm D}$  values and, hence, much better  $T_{\rm D}/T_{\rm P}$ .

Fig. 6 shows the cycling-induced degradation of  $V_{\rm TH}$  in programmed and erased states, under CHISEL (point a), SSEP (point b), and CHE (having similar  $V_{\rm D}$  as SSEP point b)

TABLE I
P/E CYCLING-INDUCED DEGRADATION OF DISTURB (CGD) TIMES IN SSEP, CHISEL (BTBT DOMINANT), AND CHE (CHANNEL LEAKAGE DOMINANT)
CONDITIONS IN EACH OF THE CELLS CYCLED USING SSEP, CHISEL, AND CHE PROGRAMMING ( $10^4$ Cycles as in Fig. 6). The Degradation in
Program/Disturb Margin Under the Different Cycling Conditions Is Also Shown

Cell	Disturb T <sub>D</sub> (s)			$T_{\rm D}/T_{\rm P} (10^6)$		
	SSEP (3.9/- 0.8)	CHISEL (3.5/- 2)	CHE (3.9/0)	SSEP	CHISEL	CHE
Virgin	2535	17.7	2.3	1207	6.6	0.8
SSEP- cycled	1185	15.3	2.3	282	-	-
CHISEL- cycled	117.6	7.4	1.6	-	2	-
CHE- cycled	58	11.8	1.2	-	-	0.2

operations. Program and erase times were always held fixed for the entire cycling period. Repeated P/E cycling creates defects at the interface and in the oxide, which can be charged and affect the charge injection during program and erase [10], [22], [23]. Electrons trapped in the oxide create a barrier for further electron injection, reducing the program speed with P/E cycling. The high-energy electrons available at higher  $|V_{\rm B}|$ values have a higher probability to be injected over this barrier, which explains the lesser degradation of programmed state  $V_{\rm TH}$ under CHISEL. After  $10^4$  P/E cycles, the degradation of both programmed and erased states under SSEP is similar compared with CHE (at the same  $V_{\rm D}$ ).

Fig. 7 shows the disturb transients before and after P/E cycling under different programming conditions (as in Fig. 6). Even after  $10^4$  P/E cycles, CGD under SSEP remains much lower than CHISEL (similar  $T_{\rm P}$ ) and CHE (similar  $V_{\rm D}$ ) programming. The interface degradation due to P/E cycling reduces the gate coupling, which, in turn, increases  $V_{\rm FG}$  for any given  $V_{\rm TH}$ . This increase in  $V_{\rm FG}$  can affect CGD by 1) increasing the area of electron injection, 2) increasing the channel leakage, and 3) decreasing the BTBT (but the trapassisted component of BTBT increases) [23]. Normally, the increase in the area of injection is dominant over the decrease in BTBT, giving a higher CGD even under CHISEL (in CHE, both the number of electrons and the area of injection increase). CGD also increases under SSEP, but it continues to be lower than for CHE or CHISEL, as both channel leakage and BTBT are kept low in SSEP. Although SSEP shows higher degradation of  $T_{\rm P}$  compared with CHISEL (as observed from the cycling window), its high  $T_{\rm D}$  ensures that  $T_{\rm D}/T_{\rm P}$  remains much larger than CHISEL even after cycling. Table I summarizes the values of  $T_{\rm D}$  and  $T_{\rm D}/T_{\rm P}$  before and after P/E cycling for the different cases considered above. Postcycling  $T_{\rm P}$  and  $T_{\rm D}$  for SSEP remain much better than those for CHE programming (at the same  $V_{\rm D}$ ).

As a further verification, the disturb transients under all the three disturb conditions are measured on each cycled cell. Due to the different origins of disturb under each disturb condition, these measurements can be used to study the effect of cycling on the individual components of the disturb. Table I also shows the  $T_D$  corresponding to SSEP, CHISEL, and CHE disturb conditions in each of the SSEP-, CHISEL-, and CHE-cycled cells. SSEP-cycled cell shows the least disturb under all



Fig. 8. Impact of technological parameters (a)  $L_{\rm FG}$  and (b)  $X_{\rm J}$  on  $T_{\rm D}$ . Scaling  $L_{\rm FG}$  increases channel leakage (low  $|V_{\rm B}|$ ) but does not affect BTBT (high  $|V_{\rm B}|$ ). Scaling  $X_{\rm J}$  decreases channel leakage and increases BTBT, shifting the minimum disturb point to a lower  $|V_{\rm B}|$ .

disturb conditions, suggesting a lower cycling-induced degradation (combined effect of both BTBT and channel leakage) compared with CHISEL- or CHE-cycled cells. Individually, the worst degradation in BTBT (channel leakage) component of disturb is observed in the cell cycled under CHISEL (CHE). These also indicate that CHISEL or CHE cycling results in a larger cell degradation than SSEP cycling, under the given bias conditions.

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## C. Impact of Technology Parameters on SSEP

The impact of technology parameters  $L_{FG}$  and  $X_{J}$  on SSEP is shown next. Channel leakage increases at lower  $L_{\rm FG}$  and higher  $X_{\rm J}$ , but BTBT is insensitive to  $L_{\rm FG}$  and increases at lower  $X_{\rm J}$ . Fig. 8(a) shows  $T_{\rm D}$  versus  $V_{\rm B}$  for different  $L_{\rm FG}$  for fixed  $X_{\rm J}$ . The optimal  $V_{\rm B}$  for minimum disturb is nearly independent of  $L_{\rm FG}$ , which only affects channel leakage. Therefore,  $T_{\rm D}$  changes with  $L_{\rm FG}$  only at low  $|V_{\rm B}|$  (channel leakage dominant) and is insensitive to  $L_{\rm FG}$  at high  $|V_{\rm B}|$  (BTBT dominant). Increase in channel leakage at lower  $L_{\rm FG}$  slightly reduces  $T_{\rm D}$ for SSEP, but the reduction in  $T_{\rm D}$  (or increase in disturb) is much smaller when compared with CHE. In addition,  $T_{\rm P}$  also reduces at lower  $L_{\rm FG}$ , ensuring little impact on program/disturb margin for SSEP operation. Fig. 8(b) shows  $T_{\rm D}$  versus  $V_{\rm B}$  for different  $X_J$  at fixed  $L_{FG}$ . Decreasing  $X_J$  reduces channel leakage but increases BTBT. Therefore, as  $X_{\rm J}$  is reduced, disturb reduces at lower  $|V_{\rm B}|$  but increases at higher  $|V_{\rm B}|$ , and the SSEP point shifts toward lower  $|V_{\rm B}|$ . Very low  $|V_{\rm B}|$  values can affect the advantages related to CHISEL that are dependent on the  $|V_{\rm B}|$  value. However, the concept of SSEP can still be used to obtain better disturb performance and higher program/ disturb margin.

## **IV. CONCLUSION**

A novel scheme to program NOR flash EEPROM cells using soft secondary electrons is introduced. SSEP uses an optimum  $V_{\rm B}$  that offers lower drain disturb compared with both CHE and conventional CHISEL conditions. The concept behind the choice of optimum  $V_{\rm B}$ , which reduces both channel leakage and BTBT under drain disturb condition, is discussed. SSEP is shown to give lower  $T_{\rm P}$  and higher  $T_{\rm D}$  than CHE for all operating conditions. It is also demonstrated that by a proper choice of  $|V_{\rm D}|$ , SSEP can give higher  $T_{\rm D}$  for similar  $T_{\rm P}$  or lower  $T_{\rm P}$  for similar  $T_{\rm D}$  (better  $T_{\rm P}/T_{\rm D}$  ratio, either way) when compared with CHISEL operation. SSEP retains the advantage even after P/E cycling and also suffers less cycling-induced degradation compared with CHISEL or CHE. SSEP offers a promising way to program scaled NOR flash EEPROMs.

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