Performance and Hot-Carrier Reliability of 100 nm Channel Length Jet Vapor Deposited Si_3N_4 MNSFETs

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***Abstract*—Metal–nitride–semiconductor FETs (MNSFETs) having channel lengths down to 100 nm and a novel jet vapor deposited (JVD) Si_3N_4 gate dielectric have been fabricated and characterized. When compared with MOSFETs having a thermal SiO_2 gate insulator, the MNSFETs show a comparable drain current drive, transconductance, subthreshold slope and pre-stress interface quality. A novel charge pumping technique is employed to characterize the hot-carrier induced interface-trap generation in MNSFETs and MOSFETs. Under identical substrate current during stress, MNSFETs show less interface-state generation and drain current degradation, for various channel lengths, stress times and supply voltages, despite the fact that the Si-Si_3N_4 barrier (2.1 eV) is lower than the Si-SiO_2 barrier (3.1 eV). The time and voltage dependence of hot-carrier degradation has been found to be distinctly different for MNSFETs compared to SiO_2 MOSFETs.**

***Index Terms*—Charge pumping, hot-carrier effect, jet vapor deposition (JVD), MOSFET, silicon nitride.**

I. Introduction

As predicted by the SIA roadmap, aggressive scaling of MOSFETs will soon result in devices having channel lengths (L) in the sub-100 nm regime [1]. To maintain performance such as speed, current drive and transconductance, the gate oxide thickness (T_{ox}) also needs to be proportionately scaled. For the present 180 nm technology node T_{ox} is close to 3 nm, and the sub-100 nm nodes beyond 2006 will require T_{ox} to be in the range of 1–2 nm [1]. However, for MOSFETs having conventional SiO_2 gate insulator, increase in direct tunneling gate leakage current is observed for gate oxide thicknesses below 3 nm [2]. It has been predicted that this leakage current will reduce gate overdrive and will result in static power dissipation, which will set a lower limit on the conventional SiO_2 thickness that can be used for sub 100 nm CMOS technologies [2], [3].

The use of high dielectric constant (k) gate insulators can significantly reduce gate leakage and alleviate the associated problems. This is due to the fact that for the same electrical oxide thickness (EOT), a higher k dielectric has a higher physical thicknesses (T_{PH}) compared to SiO_2 $(T_{PH} = k/kSiO_2 \times \mathrm{EOT})$. Several materials that have been considered for alternative gate dielectrics are silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), tantalum pentoxide (Ta_2O_5) and titanium oxide (TiO_2), having k ranging from about 7 for silicon nitride to about 30 for tantalum pentoxide. However, there are many problems associated with the use of high-k insulators, such as incompatibility with standard silicon processes, thermal instability, poor interface with silicon, low band gap, reduced conduction band offset and large densities of bulk traps.

Of the high-k materials, silicon nitride is attractive because it is readily compatible with standard silicon technology. Although its k value is only about twice that of SiO_2, that would still lead to large enough physical thicknesses for the next few technology generations (upto about 2005) to suppress direct tunneling considerably. Conventionally, silicon nitride has been deposited or grown on silicon for use as a gate insulator by either CVD [4] or direct nitridation of silicon [5]. The major problem with conventionally deposited silicon nitride as a gate insulator has been the poor quality of interface with silicon, and large number of bulk traps. Recently, jet vapor deposited (JVD) Si_3N_4 has been shown to have excellent electrical properties as a gate insulator material [6], [7]. For identical gate EOT, JVD Si_3N_4 shows more than 2–3 orders of magnitude lower gate leakage current compared to thermal SiO_2. Moreover, JVD is a low temperature process, easy to integrate in the conventional CMOS line, and provides excellent resistance to boron penetration, all of that makes it a viable candidate for replacing thermal SiO_2 as the gate insulator. However, in order to qualify as a gate insulator, the Si-Si_3N_4 interface quality should be comparable to thermal SiO_2, especially for the sub-100 nm nodes. Moreover, due to the lower Si-Si_3N_4 conduction band energy barrier (2.1 eV compared to 3.1 eV for Si-SiO_2), significant hot-carrier injection can take place in FET's having a Si_3N_4 gate insulator. Therefore, the as-grown Si-Si_3N_4 interface, its effect on pre-stress device performance and its hot-carrier reliability require detailed investigation.

In this paper, we report detailed electrical characterization results on JVD Si_3N_4 MNSFET's and conventional SiO_2 MOSFETs having channel lengths down to 100 nm. We show that MNSFETs have comparable pre-stress drain current drive, transconductance and interface quality with respect to MOSFETs. Hot-carrier degradation in these devices was studied

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using a recently developed charge pumping technique [8], which can furnish details about the generated damage profiles. Post-stress interface-state generation and the resulting drain current degradation have been studied as functions of supply voltages and stress times and on devices having different channel lengths. For stressing under identical conditions, the MNSFETs show improved hot-carrier hardness compared to MOSFETs, despite the lower energy barrier of Si-Si_3N_4.

Section II presents device fabrication and the charge pumping and device stressing schemes used for post-stress characterization. Experimental results are presented and discussed in Section III, followed by conclusions in Section IV.

II. Experimental

A. Device Fabrication

Two sets of n-channel FET's were fabricated in an identical way except for the gate insulator. E-beam lithography was used to define channel lengths down to 100 nm. One set of devices has a Si_3N_4 gate dielectric, deposited using the JVD process [6], [7], followed by annealing at 800°C for 25 min in N_2 (referred as MNSFET's). Another set of devices has SiO_2 grown at 800 °C in dry O_2, followed by an in-situ N_2 anneal (referred as MOSFETs). A two-step Ti-silicidation with Ge-preamorphization was performed to control the silicide depth and to reduce series resistance. The electrical oxide thickness (EOT) is 3.1 nm for JVD Si_3N_4 MNSFETs and 3.9 nm for SiO_2 MOSFETs, as obtained using the split CV technique in inversion [9].

B. Charge Pumping

Charge pumping (CP) was performed using fixed base and varying top level trapezoidal gate pulses having a frequency of 1 MHz and rise and fall time of 250 ns. The substrate was shorted to ground, and the dc current (the charge pumping current) was measured at the source and drain. The distributions of post-stress interface-trap density ($\Delta N_{\rm it}$) were determined by a novel data analysis scheme recently reported by us [8]. This technique does not require backup computer simulation, avoids numerical data differentiation and directly provides reliable and robust estimates of $\Delta N_{\rm it}$ profiles along the channel [8], [10]. The details of the data analysis scheme are discussed elsewhere [8].

C. Device Stressing

The MNSFETs and MOSFETs used in this study were stressed at peak substrate current condition ($V_{\rm G} = V_{\rm D}/2$). It is well known that this stress condition corresponds to maximum interface-trap generation and very little charge trapping [10], [11], and is the dominant degradation mode in transistors having thin gate insulators ($T_{\rm ox} < 4$ nm) [12]. Since charge trapping is insignificant in MOSFET's with thin gate insulators [12]–[14], these samples were not stressed at other conditions ($V_{\rm G} = V_{\rm T}$ and $V_{\rm G} = V_{\rm D}$), where $N_{\rm it}$ generation is known to be smaller [8], [10], [11]. Transfer $I_{\rm D}$-$V_{\rm G}$ (at $V_{\rm D} = 50$ mV) and charge pumping measurements were performed before and after each stress interval. Transconductance degradation was measured from I–V characteristics and interface-trap distributions was calculated from charge pumping characteristics.

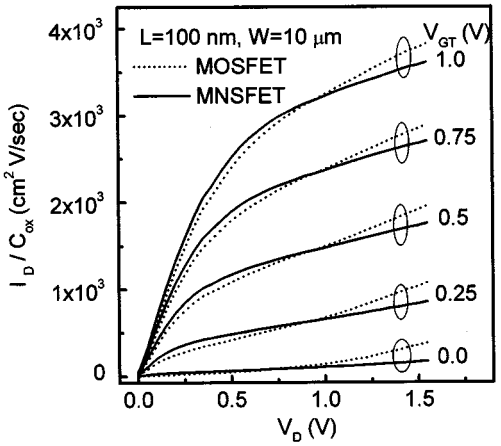

Fig. 1. Output characteristics of 100 nm channel length MNSFET and MOSFET. The drain current was measured at identical $V_{\rm G} - V_{\rm T}$ ($V_{\rm GT}$) values and normalized to gate capacitance to account for differences in gate oxide thickness.

III. Results and Discussion

A. Pre-Stress Characterization

Fig. 1 shows the output characteristics of a 100 nm channel length MNSFET and a MOSFET. Since the gate insulator thicknesses were different, the threshold voltages were slightly different: $V_{\rm T} = 0.41$ V for the MNSFET and $V_{\rm T} = 0.43$ V for the MOSFET. So, the drain current was measured at identical $V_{\rm G} - V_{\rm T}$ ($V_{\rm GT}$) values and normalized to the gate capacitance for fair comparison. It can be seen that the drain current drive of MNSFET is comparable to that of MOSFET. The pre-stress interface-trap densities ($N_{\rm it}$) of these devices were found using charge pumping. Fig. 2(a) shows the charge pumping current ($I_{\rm CP}$) as a function of pulse top level ($V_{\rm TOP}$) for a 100 nm MNSFET and a MOSFET. Similar measurements were done on identical devices having different gate length (L). As shown in Fig. 2(b), the $I_{\rm CP,\,MAX}$–L data when fitted by a straight line furnish the pre-stress average interface-trap density ($\langle N_{\rm it} \rangle$) [15]. Note that the unstressed $\langle N_{\rm it} \rangle$ is only about a factor of two higher in MNSFETs compared to MOSFETs.

Fig. 3(a) shows the normalized transconductance ($g_{\rm m}$) as a function of gate bias ($V_{\rm G}$) for a $L = 100$ nm MNSFET and MOSFET. Although the $g_{\rm m}$ at low gate biases is lower for the JVD device, it crosses over the value for SiO_2 MOSFET at higher $V_{\rm G}$'s, a fact also reported by other workers, and has been attributed to the presence of large densities of border traps in JVD Si_3N_4 [16]. Fig. 3(b) shows the saturation transconductance ($g_{\rm m\,sat}$) (at $V_{\rm GT} = V_{\rm D} = 1.5$ V) and the subthreshold slope (S) as a function of L for the MNSFETs and MOSFETs. For fair comparison, the $g_{\rm m\,sat}$ values of MNSFETs were scaled by the ratio of the gate capacitances for MOSFETs and MNSFETs used in the measurements. Note that no appreciable degradation in $g_{\rm m\,sat}$ is observed for MNSFETs. The 5% degradation in sub-threshold slope in MNSFET's compared to MOSFETs can be attributed to the slightly higher $\langle N_{\rm it} \rangle$ as shown in Fig. 2(b).

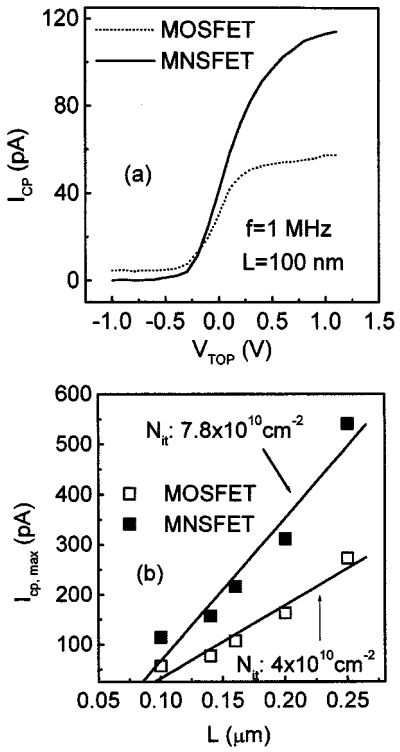

Fig. 2. (a) Pre-stress charge pumping current versus pulse top level for 100 nm channel length MNSFET and MOSFET, (b) maximum charge pumping current versus drawn channel length for MNSFET's and MOSFET's. Pulse base level was held at -2 V and $I_{\mathrm{CP,MAX}}$ was obtained at $V_{\mathrm{TOP}} = 1$ V.

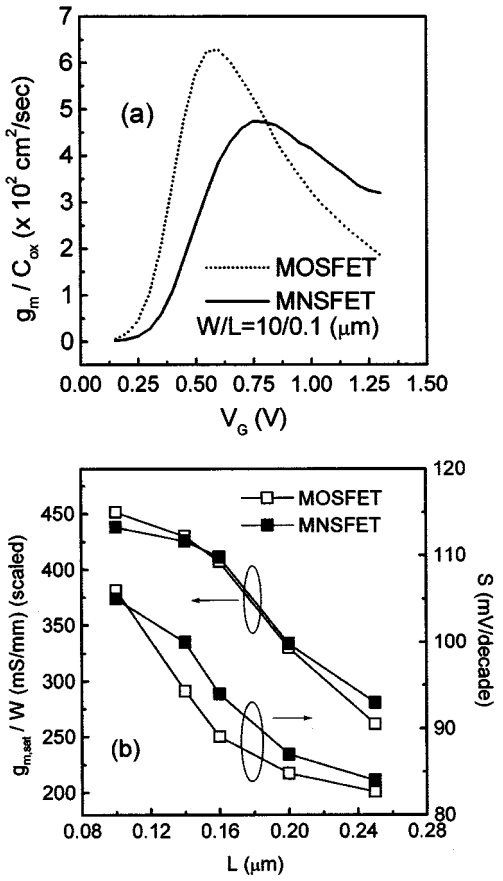

Fig. 3. (a) Transconductance versus gate voltage for 100 nm channel length MNSFET and MOSFET, (b) saturation transconductance and subthreshold slope versus channel lengths for MNSFET's and MOSFETs.

B. Post-Stress Characterization

In Fig. 4(a), the post-stress incremental CP current is shown for 100 nm MNSFET and MOSFET, stressed at $V_{\mathrm{G}} = V_{\mathrm{D}}/2$ for 1000s. Note that for identical stress V_{D}, the substrate current was found to be larger in MNSFETs due to its smaller EOT compared to the conventional devices [12], [17]. Therefore, the drain bias (V_{D}) was suitably adjusted for identical substrate currents $(I_{\mathrm{SUB}} = 41\ \mu\mathrm{A})$ during stress, which was 2.65 V and 2.8 V respectively for MNSFETs and MOSFETs. These values of stress biases were found to be moderate enough to prevent unrealistically high degradation. The resulting profiles of the generated interface traps along the channel as obtained using the novel charge pumping technique are shown in Fig. 4(b). It can be clearly seen that the stress induced CP current and the resulting ΔN_{it} profiles are lower for MNSFET compared to MOSFET.

Similar ΔN_{it} profiles were obtained on 100 nm devices stressed for different times and drain biases, and also on devices having different channel lengths. The results are shown in Figs. 5–7, where the peak magnitude $(\Delta N_{\mathrm{it,p}})$ and the spread $(\Delta\sigma)$ of the interface-trap profiles are plotted together with the resulting normalized transconductance degradation $(\Delta g_{\mathrm{m}}/g_{\mathrm{m,o}})$. Δg_{m} was calculated from transfer characteristics measured at $V_{\mathrm{D}} = 50$ mV. $\Delta\sigma$ was calculated as the portion of the channel where the condition $\Delta N_{\mathrm{it}} > 5 \times 10^{10}\ (\mathrm{cm}^{-2})$is satisfied [10], [12]. Note that this choice of the cutoff value for calculating $\Delta\sigma$ is somewhat arbitrary, and a different cutoff value would result in a different value of $\Delta\sigma$. However, we have verified that the trends in $\Delta\sigma$ remain independent of the choice of this cutoff value [18]. The following discussions, based mostly on relative damage magnitude and its trends, therefore do not critically depend on the exact values of $\Delta\sigma$. Note that instead of using full width at half maximum, this definition of $\Delta\sigma$ estimates the length of the degraded part of the channel, irrespective of the peak magnitude of damage.

Fig. 5 shows the time evolution of $\Delta N_{\mathrm{it,p}}$, $\Delta\sigma$ and $\Delta g_{\mathrm{m}}/g_{\mathrm{m,o}}$ for a 100 nm channel length MNSFET and MOSFET. As before, due to the difference in EOT, the drain bias was adjusted for peak $I_{\mathrm{SUB}} = 41\ \mu$A during stress. Note that in both types of devices, $\Delta N_{\mathrm{it,p}}$ and Δg_{m} follow a t^n dependence with stress time, while $\Delta\sigma$ show a $A\log(t)$ dependence, in accordance with previously reported results [10], [19]. $\Delta N_{\mathrm{it,p}}$ and $\Delta\sigma$ are found to be lower in MNSFET for all stress times, with a lower rate of buildup ($n = 0.25$ and $A = 11$ nm/decade) compared to that of MOSFET ($n = 0.47$ and $A = 16$ nm/decade). Since both the peak and the spread of the interface trap profiles affect the drain current [10], [12], both the slope and magnitude of Δg_{m} are found to be lower in MNSFETs $(n = 0.28)$ compared to MOSFETs $(n = 0.49)$. The possible reasons for reduced interface-trap generation in MNSFET is discussed later.

Fig. 6 shows $\Delta N_{\mathrm{it,p}}$, $\Delta\sigma$and $\Delta g_{\mathrm{m}}/g_{\mathrm{m,o}}$ as a function of stress drain bias for 100 nm channel length MNSFET's and MOSFETs, stressed at $V_{\mathrm{G}} = V_{\mathrm{D}}/2$ condition for 100 s. Note that stressing at different drain biases were performed on different but identical transistors located at adjacent dies in the wafer. For realistic comparison, $\Delta N_{\mathrm{it,p}}$, and $\Delta\sigma$ for

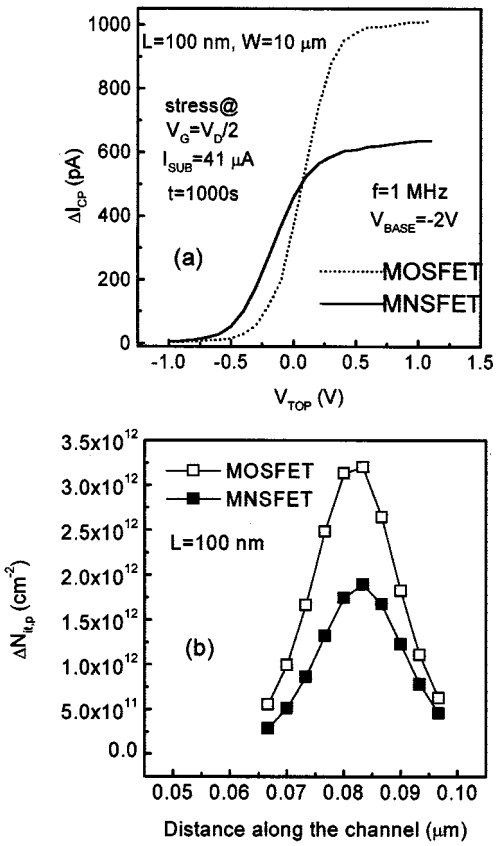

Fig. 4. (a) Post-stress incremental charge pumping current versus pulse top level and (b) generated interface-trap density profile along the channel for 100 nm channel length MNSFET and MOSFET.

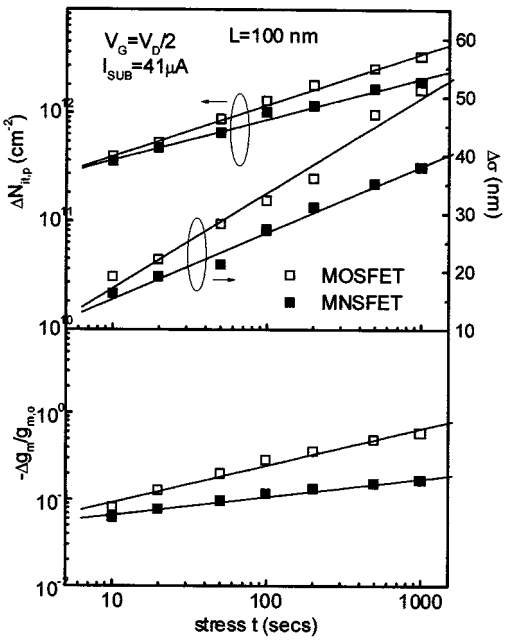

Fig. 5. Peak magnitude and spread of interface-trap profiles, and transconductance degradation as a function of stress time for 100 nm channel length MNSFET and MOSFET. Stressing was done at maximum substrate current condition.

MNSFET were obtained by normalizing the incremental CP current (ΔI_{CP}) by the ratio of $I_{\rm SUB}$ measured for MOSFET

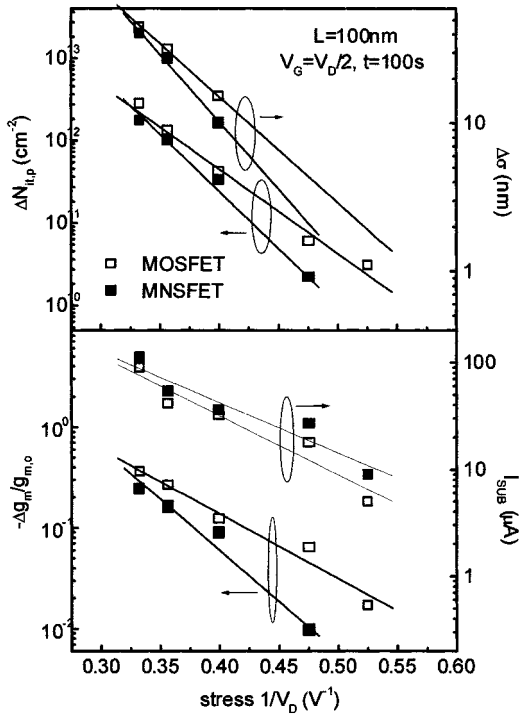

Fig. 6. Peak magnitude, spread of interface-trap profiles, transconductance degradation and initial $I_{\rm SUB}$ as a function of stress drain bias for 100 nm channel length MNSFET and MOSFET. Stressing was done at maximum substrate current condition.

and MNSFET during stressing at each bias point, i.e., $\Delta I_{\rm CP}$(MNSFET,normalized) $=\Delta I_{\rm CP}$(MNSFET,measured) $\times$ $\{I_{\rm SUB}$(MOSFET, measured)$/I_{\rm SUB}$(MNSFET,measured)$\}$. The $\Delta g_{\rm m}$ values were also identically normalized, i.e., $\Delta\Delta g_{\rm m}$(MNSFET,normalized) $=\Delta g_{\rm m}$(MNSFET,measured) $\times$ $\{I_{\rm SUB}$(MOSFET, measured). It can be seen that $\Delta N_{\rm it,p}$, $\Delta\sigma$and hence $\Delta g_{\rm m}$ follow an $\exp(-\alpha/V_{\rm D})$ dependence, which can be attributed to similar dependence of substrate current on drain bias [20]. We have found $\alpha = 22$ V and 32 V for $\Delta N_{\rm it,p}$, 8.9 V and 12.4 V for $\Delta\sigma$,and 25 V and 33.2 V for $\Delta g_{\rm m}$, respectively for MOSFET's and MNSFETs. Note that $\Delta N_{\rm it,p}$, $\Delta\sigma$and hence $\Delta g_{\rm m}$ are significantly lower in MNSFETs for low and moderate $V_{\rm D}$ values, though the difference diminishes at higher $V_{\rm D}$ values. This indicates that at not so high drain bias, though the presence of the number of energetic carriers are more in Si_3N_4 films (due to lower energy barrier), the Si-Si_3N_4 interface is more resistant to interface-state generation compared to the Si-SiO_2 interface. However, since carrier injection probability is exponentially dependent on carrier energy (hence $V_{\rm D}$) [21], carrier injection becomes much higher in Si_3N_4 films at high $V_{\rm D}$ and has a competing effect, resulting in identical degradation for MNSFETs and MOSFETs. However, the key point is the significant improvement in the HCD performance for MNSFETs over MOSFETs at lower $V_{\rm D}$ values, pertinent to devices in the sub 100 nm channel length regime.

Fig. 7 shows $\Delta N_{\rm it,p}$, $\Delta\sigma$ and $\Delta g_{\rm m}/g_{\rm m,o}$ as functions of channel length. The stressing was performed at $V_{\rm G} = V_{\rm D}/2 = 1.4$ V for 100 s. As discussed before, the $\Delta N_{\rm it,p}$, and $\Delta\sigma$ for MNSFETs were obtained by normalizing the incremental CP current by the ratio of $I_{\rm SUB}$ measured

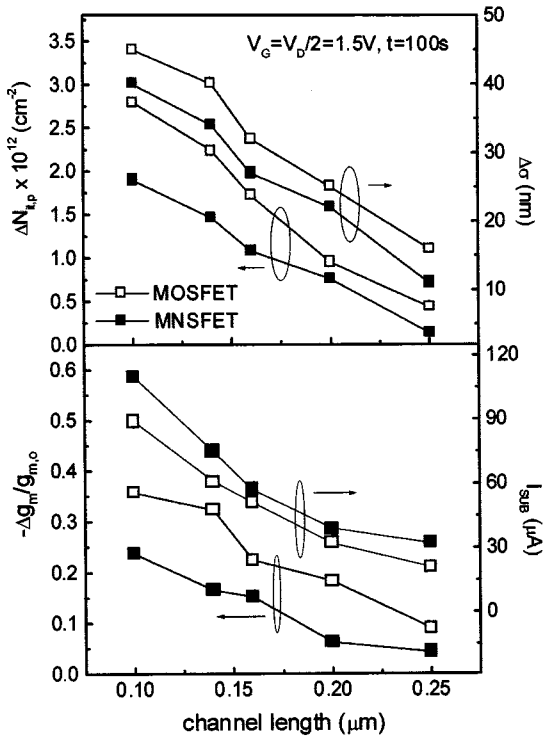

Fig. 7. Peak magnitude, spread of interface-trap profiles, transconductance degradation and initial $I_{\rm SUB}$ as a function of channel length for MNSFET and MOSFET. Stressing was done at maximum substrate current condition.

for MOSFET and MNSFET during stressing. The $\Delta g_{\rm m}$ values were also identically normalized. It can be again seen that $\Delta N_{\rm it,p}$, $\Delta\sigma$ and hence the resulting $\Delta g_{\rm m}$ is lower in MNSFET's for all channel lengths used in the study. Also shown in Figs. 6 and 7 are the initial $I_{\rm SUB}$ values for different drain biases and channel lengths. $I_{\rm SUB}$ is slightly higher for the MNSFETs compared to MOSFETs, and this is mainly due to the smaller EOT of the JVD nitride compared to the oxide.

Note that the relative degradation between MNSFETs and MOSFETs depends on the choice of stress time (Fig. 5) and stress $V_{\rm D}$ (Fig. 6). Moreover, MNSFETs and MOSFETs show almost identical degradation at very high $V_{\rm D}$ values (Fig. 6). In the present case, the stress voltages were chosen as close as possible to the normal operating biases so as to prevent unrealistically high degradation. Note that a different stress drain bias and/or time will lead to a different amount of degradation. Once again, the key point is the significant improvement in the HCD performance for MNSFET's over MOSFET's at $V_{\rm D}$ values pertinent in the 0.1–0.25 μm nodes. Due to the lower drain bias during actual operation compared to that during stress, the degradation in MNSFETs will be much lower than shown, as is evident from Fig. 6.

The mechanism for interface-state generation is most commonly described by either the proton (H^+) drift [21] or the trapped-hole recombination (THR) [22] models. We speculate that the improvement seen in our MNSFETs points to the THR mechanism, since the lower bandgap for Si_3N_4 would give rise to less energy release during recombination, and therefore fewer interface states. However, further studies are needed before the exact mechanisms at work can be explicated.

IV. Conclusion

To summarize, MNSFETs having channel lengths down to 100 nm and a JVD Si_3N_4 gate dielectric have been fabricated and characterized. Compared to conventional SiO_2 MOSFETs, the MNSFETs show very similar drain current drive, transconductance and subthreshold slope. Charge pumping measurements in pre-stress show as-grown interface traps in MNSFETs are only twice as large as in conventional devices. A novel charge pumping technique was used to determine the stress-induced interface trap profiles in devices subjected to hot-carrier stress. It was shown that both the peak $(\Delta N_{\rm it,p})$ and spread $(\Delta\sigma)$ of the generated interface-trap profiles as well as the transconductance degradation $(\Delta g_{\rm m})$ are lower in MNSFETs compared to MOSFETs, as functions of supply voltage, stress time and for all channel lengths. With variation in stress time, $\Delta N_{\rm it,p}$ and $\Delta g_{\rm m}$ show a t^n dependence, while $\Delta\sigma$ goes as $A\log(t)$, and both the magnitude and rate of damage buildup are lower in MNSFETs. With variation in drain bias, $\Delta N_{\rm it,p}$, $\Delta\sigma$ and hence $\Delta g_{\rm m}$ follow an $\exp(-\alpha/V_{\rm D})$ dependence, the damage buildup being suppressed more in MNSFETs at lower drain bias. This study therefore indicates that compared to conventional SiO_2 MOSFETs, the JVD Si_3N_4 MNSFET's show 1) comparable pre-stress interface quality and electrical performance, and 2) improved hot-carrier hardness. Hence the MNSFETs have the potential to be excellent candidates for future sub 100 nm CMOS technology.

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